

## LOW $I_Q$ , 30 $\mu$ A, HIGH $V_{IN}$ QUAD-OUTPUT POWER SUPPLY

Check for Samples: [TPS43340-Q1](#), [TPS43341-Q1](#)

### FEATURES

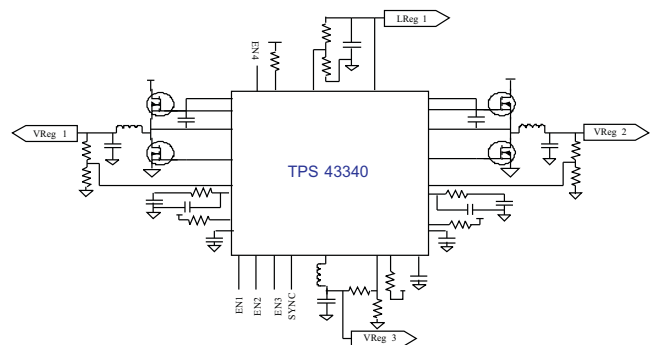
- **Input Voltage Range: 4 V to 40 V, Transients up to 60 V**
- **Dual Output Synchronous Buck Controller**
  - Peak Gate Drive Current 0.6 A
  - Separate Enable Inputs (EN1, EN2)
  - Automatic Low-Power Mode Operation
  - Low Current Consumption
    - 30  $\mu$ A (Typ) With Single Output Operation in Low Power Mode
    - 35  $\mu$ A (Typ) With Dual Output Operation in Low Power Mode
- **Low Shutdown Current,  $I_{sh} = 5 \mu$ A Typ**
- **Single Synchronous Buck Regulator Converter BUCK3**
  - Max Output Current 2 A
  - Enable Input EN3
- **Linear Regulator LREG1**
  - Enable Input EN4
- **Internal Oscillator, Programmable via External Resistor, 150 kHz to 600 kHz for Switching Frequency  $f_{SW\_BUCK1,2,3}$**
- **Integrated PLL, External Synchronization Frequency: 150 kHz to 600 kHz**
- **Switch Mode Regulators Operate with 180° Phase-Shift**
- **Pseudo Random Frequency Hopping Spread Spectrum**
- **Soft Start Input for Switchmode Supplies (SS1, SS2, SS3)**
- **Reset Output for All Output Rails**

- **Reset Delay, Programmable with Capacitor**
- **Supply Under Voltage/Over Voltage Detection and Shutdown**
- **Short Circuit, Over Current, and Thermal Protection on Buck Regulator Gate Drive, Buck Reg Converter, and Linear Regulator Output**
- **Internal Thermal Overload Protection**
- **Thermally Enhanced PowerPAD™ Package**
  - 48-Pin HTQFP (PHP)

### APPLICATIONS

- Infotainment
- Navigation
- TFT Cluster Display
- Automotive ECU
- Advanced Driver Information Systems
- Multi Rail DC Power Distribution Systems

Simplified Schematic



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION

The TPS43340/1 is a dual buck regulator controller (BUCK1, BUCK2), single Buck regulator converter (BUCK3) and linear regulator (LREG1) designed for powering the Texas Instruments family of DSPs and Microcontrollers or general market MCU products. The device features integrated short-circuit and over-current protection on the gate drive outputs for the Buck regulator controllers. Independent current fold back control for each Buck regulator supply during regulator output short to ground. A soft start is incorporated on each output supply to ensure on initial power up these regulated outputs are not in current limit. Reset delay is implemented on power up to allow the outputs of BUCK1, BUCK2, BUCK3 and Linear regulator to get to stable regulation. The delay is programmed with an external capacitor to a maximum range of 300 ms. Each power supply output has adjustable output voltage based on the external resistor network settings. The device has sequencing control during power up and down of the output rails based on the enable/disable control or soft start.

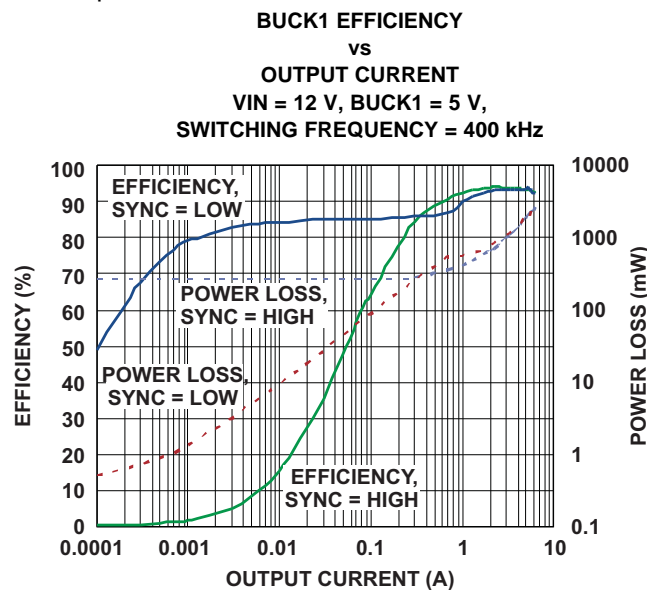


Figure 1.

## ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	SPREAD SPECTRUM	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER
-40°C to 125°C	OFF	HTQFP - PHP	TPS43340QPHPRQ1
	ON		TPS43341QPHPRQ1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

			MIN	MAX	UNIT
Supply inputs	Input voltage	VIN	-0.3	60	V
Buck controller Buck1 and Buck2	Enable inputs	EN1, EN2	-0.3	60	V
	Bootstrap supplies	BOOT1, BOOT2	-0.3	68	V
	Phase inputs	PH1, PH2	-1.0	60	V
		PH1, PH2 (for 100 ns)	-2.0		V
	Feedback inputs	VSENSE1, VSENSE2	-0.3	13	V
	Error amplifier outputs	COMP1, COMP2	-0.3	13	V
	External MOSFET driver peak output currents	GU1, GU2, GL1, GL2		1.0	A
	External MOSFET driver	GL1-PGND1, GL2-PGND2	-0.3	8.8	V
		GU1-PH1, GU2-PH2	-0.3	8.8	V
	Current sense voltage	S1, S2, S3, S4	-0.3	13	V
	Absolute differential Voltage	S1-S2 ,  S3-S4		2	V
	Soft start	SS1, SS2	-0.3	13	V
	Power good outputs	RST1, RST2	-0.3	13	V
	Switching frequency oscillator	RT	-0.3	13	V
	External input clock	SYNC	-0.3	13	V
External input supply for gate drive	EXTSUP	-0.3	13	V	
Buck converter Buck3	Input supply	VSUP	-0.3	13	V
	Slew rate setting	SLEW	-0.3	13	V
	Enable input	EN3	-0.3	13	V
	Bootstrap supply	BOOT3	-1	20	V
	Phase inputs	PH3	-1	13	V
		PH3 (for 100 ns)	-2		V
	Feedback input	VSENSE3	-0.3	13	V
	Soft start	SS3	-0.3	13	V
	Power good output	RST3	-0.3	13	V
Error amplifier output	COMP3	-0.3	13	V	
Linear regulator LREG1	Input voltage	VLR1	-0.3	60	V
	Output voltage	LREG1	-0.3	7	V
	Enable input	EN4	-0.3	60	V
	Power good output	RST4	-0.3	8.8	V
	Feedback inputs	VSENSE4	-0.3	13	V
GPULL, Rdelay, VREG, VIN2SENSE	PMOS driver	GPULL	-0.3	60	V
	Zener clamp current	GPULL		0.2	mA
	Internal regulator	VREG	-0.3	8.8	V
	Reset delay	Rdelay	-0.3	8.8	V
	Feedback input	VIN2SENSE	-0.3	60	V
Temperature	Junction temperature: T <sub>J</sub>		-40	150	°C
	Operating temperature: T <sub>A</sub>		-40	125	°C
	Storage temperature: T <sub>S</sub>		-55	165	°C
	Lead temperature (Soldering 10sec)			260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to GND.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup> (continued)**

			MIN	MAX	UNIT
Electrostatic discharge ratings (ESD)	Human Body Model (HBM)	except VLR1		±2	kV
		VLR1		±1	kV
	Machine Model (MM)	except RSTx		±200	V
		RSTx		±100	V
	Charged Device Model (CDM)	all pins		±500	V
		corner pins		±750	V

**RECOMMENDED OPERATING CONDITIONS**

			MIN	MAX	UNIT
Supply inputs	Input voltage	VIN	4	40	V
Buck controller Buck1 and Buck2	Enable inputs	EN1, EN2	0	40	V
	Bootstrap inputs	BOOT1, BOOT2	4	48	V
	Phase inputs	PH1, PH2	-0.6	40	V
		PH1, PH2 (for 50 ns)	-2.0		V
	Feedback inputs	VSENSE1, VSENSE2	0	6	V
	Error amplifier outputs:	COMP1, COMP2	0	6	V
	External MOSFET driver peak output currents	GU1, GU2, GL1, GL2		0.75	A
	Current sense voltage	S1, S2, S3, S4	0	11	V
	Soft start	SS1, SS2	0	6	V
	Power good outputs	RST1, RST2	0	11	V
	Switching frequency setting	RT	0	1.2	V
	External input clock	SYNC	0	9	V
	External input supply for gate drive	EXTSUP	0	9	V
Buck converter Buck3	Input supply	VSUP	4	10	V
	Slew rate setting	SLEW	0	VREG	V
	Enable input	EN3	0	6	V
	Boot inputs	BOOT3	0	18	V
	Phase inputs	PH3	-1	11	V
		PH3 (for 50 ns)	-2		V
	Feedback input	VSENSE3	0	6	V
	Soft start	SS3	0	6	V
	Power good output	RST3	0	11	V
Error amplifier output	COMP3	0	6	V	
Linear regulator LREG1	Input voltage	VLR1	4	40	V
	Output voltage	LREG1	0.8	5.25	V
	Enable input	EN4	0	40	V
	Power good output	RST4	0	5.25	V
	Feedback inputs	VSENSE4	0	6	V
PMOS driver	PMOS driver	GPULL	4	40	V
	Internal regulator	VREG	0	6	V
Temperature ratings	Thermal resistance junction to ambient <sup>(1)</sup> , $\theta_{JA}$			31	°C/W
	Thermal resistance junction to pad <sup>(2)</sup> , $\theta_{JC}$			1.8	°C/W
	Operating temperature, $T_A$		-40	125	°C

(1) This assumes a JEDEC JESD 51-5 standard board with thermal vias – See *PowerPad™ Thermally Enhanced Package* application note from Texas Instruments (TI literature number [SLMA002](#)) for more information.

(2) This assumes junction to exposed pad.

## ELECTRICAL CHARACTERISTICS

VIN = VLR1 = 8 V to 18 V, VSUP = 4 V to 10 V, T<sub>J</sub> = -40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test <sup>(1)</sup>
<b>Input Supply</b>							
VIN	Device operating range	Input voltage required for device on initial start up	6.5		40	V	PT
		Operating range after initial start up	4.0			V	
VIN <sub>UV</sub>	Undervoltage lockout	VIN falling	3.5	3.6	3.8	V	PT
		VIN rising		3.8	4	V	
VLR1	Device operating range for linear reg	Recommended operation range	4.0		40	V	PT
I <sub>q_LPM</sub>	LPM quiescent current: T <sub>A</sub> = 25°C	EN1 = 1, LPM; EN2,3,4 = 0		30	40	μA	PT
		EN2 = 1, LPM; EN1,3,4 = 0					
		EN4 = 1, LPM; EN1,2,3 = 0		48	60		
		EN1,2 = 1, LPM; EN3,4 = 0		35	45	mA	
		EN3,4 = 1, EN2,3 = 0		4	4.5		
I <sub>q_LPM</sub>	LPM quiescent current: T <sub>A</sub> = 125°C	EN1 = 1, LPM; EN2,3,4 = 0		40	50	μA	PT
		EN2 = 1, LPM; EN1,3,4 = 0					
		EN4 = 1, LPM; EN1,2,3 = 0		52	60		
		EN1,2 = 1, LPM; EN3,4 = 0		40	45	mA	
		EN3,4 = 1, EN2,3 = 0		5			
I <sub>VIN</sub>	Quiescent current: T <sub>A</sub> = 25°C	VIN = 13 V, Buck1: CCM, Buck2: off or VIN = 13 V, Buck2: CCM, Buck1: off or VIN = 13 V, Buck1/2: CCM		5		mA	PT
I <sub>VIN</sub>	Quiescent current: T <sub>A</sub> = 125°C	Normal operation, SYNC = 5 V		5		mA	PT
		VIN = 13V, Buck1: CCM, Buck2: off		5			
		VIN = 13V, Buck2: CCM, Buck1: off		5			
		VIN = 13V, Buck1, 2: CCM		7			
I <sub>VIN-SD</sub>	Shutdown current at T <sub>A</sub> = 25°C	EN1,2,3,4 = 0: off, VIN = VLR1 = 13 V		5	10	μA	PT
I <sub>VIN-SD</sub>	Shutdown current at T <sub>A</sub> = 125°C	EN1,2,3,4 = 0: off, VIN = VLR1 = 13 V			20	μA	PT
I <sub>VLR1-SD</sub>	Shutdown current at T <sub>A</sub> = 125°C	EN1,2,3,4 = 0: off, VIN = VLR1 = 13 V			5	μA	PT
<b>Internal Supply VREG</b>							
V <sub>REG</sub>	Internal regulated supply	VIN = 8 V to 18 V, EXTSUP = 0 V, SYNC = High	5.5	5.8	6.1	V	PT
	Load regulation	EXTSUP = 0 V, SYNC = High I <sub>VREG</sub> = 0 mA to 100 mA		0.2	1	%	PT
V <sub>REG-EXTSUP</sub>	Internal regulated supply	EXTSUP = 8.5 V, normal mode	7.2	7.5	7.8	V	PT
	Load regulation	EXTSUP = 8.5 V to 13 V, normal mode I <sub>VREG</sub> = 0 mA to 125 mA		0.2	1	%	PT
V <sub>EXTSUP-VREG</sub>	Switch over voltage	I <sub>VREG</sub> = 0 mA to 100 mA, EXTSUP ramping positive, normal mode	4.4	4.6	4.8	V	PT
V <sub>EXTSUP-HYS</sub>	Switch over hysteresis	Normal mode	150		250	mV	PT
I <sub>REG-LIM</sub>	Current limit on VREG	EXTSUP = 0 V normal mode as well as LPM, VREG=0V	100		400	mA	PT
I <sub>REG-EXTSUP-LIM</sub>	Current limit on VREG when using EXTSUP	I <sub>VREG</sub> = 0 mA to 100 mA, EXTSUP = 8.5 V, normal mode, VREG=0V	125		400	mA	PT
<b>Input voltage VIN - Overvoltage Lock Out and Reverse Polarity Protection</b>							
V <sub>OVLO</sub>	Overvoltage shutdown	VIN rising	45	46	47	V	PT
		VIN falling	43	44	45	V	
OVLO <sub>Hys</sub>	Hysteresis		1	2	3	V	PT
OVLO <sub>filter</sub>	Filter time			5		μs	Info
V <sub>GD</sub>	Clamping voltage of ext. FET	VIN - GPULL		17		V	Info
R <sub>GPULL</sub>	Internal resistance to GND			500		kΩ	Info

- (1) PT: Production Tested  
 CT: Characterization Only, NOT Production Tested  
 Info: Information only, NOT production tested

## ELECTRICAL CHARACTERISTICS (continued)

VIN = VLR1 = 8 V to 18 V, VSUP = 4 V to 10 V, T<sub>J</sub> = -40°C to 150°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	Test <sup>(1)</sup>
<b>Buck Controllers</b>							
V <sub>Buck1/2</sub>	Adjustable output voltage range	Closed loop	0.9		11	V	PT
V <sub>ref</sub>	Internal reference voltage	VSENSE1/2 pin, load = 0 mA	0.792	0.800	0.808	V	PT
		Internal tolerance on reference	-1		1	%	Info
V <sub>ref, LPM</sub>	Internal reference voltage in low power mode	VSENSE1/2 pin, load = 0 mA	0.784	0.800	0.816	V	PT
		Tolerance	-2		2	%	Info
V <sub>sense</sub>	Maximum peak forward current sense voltage in CCM	S1-S2 respectively S3-S4 VSENSEx = 0.75 V, low duty cycles	60	75	90	mV	PT
	Minimum peak forward current sense voltage in CCM	S1-S2 respectively S3-S4 VSENSEx = 1 V	-65	-37.5	-23	mV	PT
V <sub>I-Foldback</sub>	Maximum peak forward current sense voltage during output short	S1-S2 respectively S3-S4 VSENSEx = 0V (foldback)	17	43.8	48	mV	CT
t <sub>dead</sub>	Shoot through delay, blanking time			20		ns	Info
DC <sub>NRM</sub>	Minimum on time	High side minimum on time		100		ns	CT
	Duty cycle	Maximum duty cycle		98.75		%	Info
DC <sub>LPM</sub>	Duty cycle LPM				80	%	CT
I <sub>LPM_Entry</sub>	LPM entry threshold load current as fraction of maximum set load current	The exit threshold is specified to be always higher than entry threshold		1		%	Info
V <sub>LPM_Exit</sub>	LPM exit threshold load current as fraction of maximum set load current			10		%	Info
<b>High-Side External NMOS Gate Drivers for Buck Controllers</b>							
I <sub>GUx_peak</sub>	Gate driver peak current			0.6		A	Info
R <sub>DS_ON</sub>	Source and sink driver	I <sub>VREG</sub> = 5.8 V, I <sub>GUx</sub> current = 200 mA		5		Ω	PT
<b>Low-Side NMOS Gate Drivers for Buck Controllers</b>							
I <sub>GLx_peak</sub>	Gate driver peak current			0.6		A	Info
R <sub>DS_ON</sub>	Source and sink driver	V <sub>REG</sub> = 5.8V, I <sub>GLx</sub> current = 200 mA		5		Ω	PT
<b>Internal Oscillator (RT)</b>							
f <sub>SW</sub>	Buck switching frequency	RT pin: GND	360	400	440	kHz	PT
f <sub>SW</sub>	Buck switching frequency	RT pin: 60 kΩ external resistor	360	400	440	kHz	PT
f <sub>SW-adj</sub>	Buck adjustable range	Using external resistor on RT (see equation)	150		600	kHz	PT
f <sub>sync</sub>	Buck synch. range	External clock input on SYNC	150		600	kHz	PT
Δf <sub>SS</sub>	Spread spectrum range	TPS43341-Q1 only, internal oscillator		±5		%f <sub>SW</sub>	PT
V <sub>RT</sub>	Oscillator reference voltage			1.2		V	PT
f <sub>SW-Prop dly</sub>	SYNC rising edge to PH rising edge delay		0	20	40	ns	Info
f <sub>SW-Trans-delay</sub>	Last SYNC rising edge to return to resistor mode if CLK is not present on SYNC pin			20		μs	Info
<b>Error Amplifier (OTA) for Buck Controllers and Buck Converter</b>							
I <sub>PULLUP_VSENSEx</sub>	Pull-up current at VSENSEx pins	VSENSEx = 0 V	50	100	200	nA	PT
gm	Forward transconductance	COMP1, COMP2 = 0.8 V; source/sink = 5 μA, Test in feedback loop	0.7	0.9	1.35	mS	PT

**ELECTRICAL CHARACTERISTICS (continued)**

 VIN = VLR1 = 8 V to 18 V, VSUP = 4 V to 10 V, T<sub>J</sub> = -40°C to 150°C (unless otherwise noted)

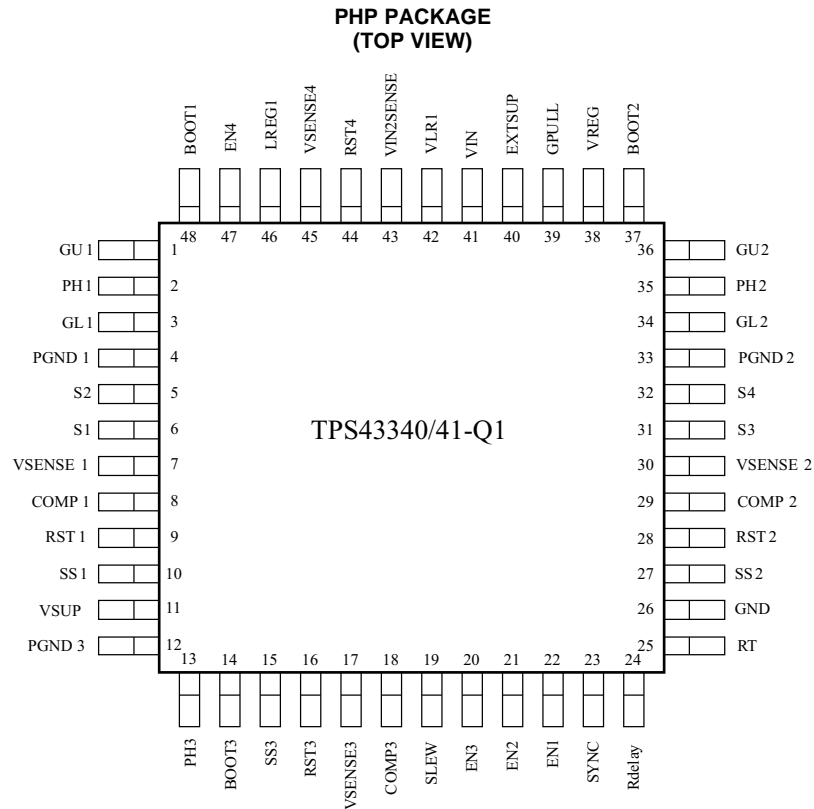
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	Test <sup>(1)</sup>	
<b>External Clock and Enable Inputs: SYNC, EN1, EN2, EN3, EN4</b>									
V <sub>IH</sub>	Higher threshold	VIN = 13 V		1.7			V	PT	
V <sub>IL</sub>	Lower threshold	VIN = 13 V				0.7	V	PT	
R <sub>IH</sub>	Pull-down resistance	VSYNC = 5 V, SYNC pull-down resistance		500			kΩ	PT	
I <sub>IL_ENx</sub>	Pull-up current	VENx = 0V ENx pull up current source		0.5		2	μA	PT	
<b>Linear Regulator LREG1</b>									
V <sub>LREG1</sub>	Regulated output range	I <sub>L</sub> = 10 μA to 300 mA		0.8		5.25	V	PT	
V <sub>Ref</sub>	Internal reference voltage tolerance	Referred to 0.8 V V <sub>REF</sub> , measured at VSENSE4		-2.5		2.5	%	PT	
V <sub>line-reg</sub>	Line reg	VIN = VLR1: 6 V to 28 V, I <sub>OUT4</sub> = 10 mA,	ΔV <sub>OUT</sub> , Vout = 5 V			15	mV	PT	
			ΔV <sub>OUT</sub> , Vout = 3.3 V			15			
			ΔV <sub>OUT</sub> , Vout = 1.5 V			15			
V <sub>load-reg</sub>	Load reg	I <sub>OUT4</sub> = 10 mA to 300 mA, VIN = 14 V	ΔV <sub>OUT</sub> , Vout = 5 V			10	mV	PT	
			ΔV <sub>OUT</sub> , Vout = 3.3 V			10			
			ΔV <sub>OUT</sub> , Vout = 1.5 V			10			
V <sub>Dropout</sub>	Drop out voltage	VIN = VLR1 = 4 V: Iout = 250 mA			500	mV	PT		
		VIN = 9 V, VLR1 = 4 V: Iout = 150 mA			300				
I <sub>OUT4</sub>	Output current	V <sub>OUT</sub> in regulation		0.01		300	mA	PT	
I <sub>LREG1-CL</sub>	Output current limit	V <sub>OUT</sub> = 0 V		400		1000	mA	PT	
d <sub>VLREG1/dt</sub>	Output soft start slew rate	Response of regulator on enable I <sub>OUT</sub> = 0 to Iout (max)				5	V/ms	PT	
PSRR	Power supply ripple rejection	V <sub>ripple</sub> = 0.5 V <sub>PP</sub> , I <sub>OUT</sub> = 300 mA	Freq = 100 Hz			60	dB	CT	
			Freq = 150 kHz			25			
C <sub>OUT4</sub>	Output capacitor range	Ceramic capacitor, C <sub>OUT_ESR</sub> = 10 mΩ to 1 Ω		1		47	μF	Info	
V <sub>TH-CP ONP</sub>	Charge pump turn-off voltage	VIN rising				9.4	V	Info	
	Hysteresis					0.18	V		
I <sub>TH-CP-OFF</sub>	Low load current detection threshold	I <sub>OUT4</sub> falling				2	mA	Info	
		Hysteresis				4			
<b>Soft Start SSx</b>									
I <sub>SSx</sub>	Soft start source current	SSx = 0 V		0.75		1	1.25	μA	PT
<b>Reset RSTx</b>									
RST <sub>pullup</sub>	RST1, RST2, RST4 Pullup	Internal pullup to S2 respectively S4, LREG1				50	kΩ	PT	
RST <sub>Xth1</sub>	Reset threshold	VSENSE <sub>x</sub> falling		-5		-7	-9.5	%VREF	PT
RST <sub>Xhys</sub>	Hysteresis					2	%VREF	PT	
RST <sub>Xdrop</sub>	Voltage drop	I <sub>RSTx</sub> = 5 mA				450	mV	PT	
		I <sub>RSTx</sub> = 1 mA				100	mV	PT	
RST <sub>Xleak</sub>	Leakage	V <sub>S2</sub> = V <sub>S4</sub> = V <sub>RSTx</sub> = 13 V / 8V for RST4				1	μA	PT	
t <sub>deglitch</sub>	Deglintch time	Power good deglitch		2		16	μs	PT	
t <sub>delay</sub>	Reset release delay	External capacitor = 1 nF				1	ms	PT	
t <sub>delay_fix</sub>	Fixed reset delay	No external capacitor, Rdelay pin open				20	50	μs	PT
I <sub>oh</sub>	Charge current source	Current to charge external capacitor		30		40	50	μA	PT
I <sub>il</sub>	Discharge current sink	Current to discharge external capacitor		30		40	50	μA	PT

## ELECTRICAL CHARACTERISTICS (continued)

VIN = VLR1 = 8 V to 18 V, VSUP = 4 V to 10 V, T<sub>J</sub> = -40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test <sup>(1)</sup>
<b>Synchronous Buck Converter VBUCK3</b>							
VSUP	VBUCK3 supply voltage		4		10	V	PT
VSUP <sub>UV</sub>	VBUCK3 undervoltage lockout	VSUP falling	3.6	3.7	3.8	V	PT
		VSUP rising	3.7	3.8	3.9	V	PT
R <sub>DS(on)</sub>	High-side switch	VSUP = 9 V, V <sub>Boot3 -PH3</sub> = 5.8 V		0.14	0.28	Ω	PT
	Low-side switch	VSUP = 9 V, V <sub>VREG-PGND3</sub> = 5.8 V		0.15	0.28	Ω	PT
I <sub>HS-Limit</sub>	High-side switch	DC test	2.5			A	PT
I <sub>LS-Limit</sub>	Low-side switch	DC test, current into PH3	2.38			A	PT
V <sub>SUPLkg</sub>	VSUP leakage current	VSUP = 10 V for high side, EN3 = Low. T <sub>J</sub> = 100°C		1		μA	PT
I <sub>FB3</sub>	Current foldback	VSENSE3 = 0 V		1.9		A	CT
f <sub>SW-adj</sub>	Buck3 switching freq range	Using external resistor on RT/CLK	150		600	kHz	PT
V <sub>Sense</sub>	Feedback voltage	Internal ref = 0.8 V	-1.5		1.5	%	PT
f <sub>SW-f-back</sub>	2-times - frequency foldback exit threshold	VSENSE3 rising		0.65		V	PT
	2-times - frequency foldback entry threshold	VSENSE3 falling		0.60			
G <sub>m3</sub>	Current loop transconductance	ΔI <sub>peakPH3</sub> /ΔV <sub>COMP3</sub>		5.4		S	CT
DC <sub>3</sub>	Minimum duty cycle	f <sub>SW</sub> = 400 kHz, SLEW = LOW or OPEN		10		%	CT
	Maximum duty cycle			98.75		%	CT
T <sub>OT-BUCK3</sub>	Overtemperature sensor	BUCK3 FETs deactivate threshold		170		°C	CT
		Hysteresis		15			
<b>Thermal Shutdown</b>							
T <sub>shutdown</sub>	Shutdown threshold	Junction temperature	150	170		°C	CT
T <sub>hys</sub>		Hysteresis		15		°C	CT

## DEVICE INFORMATION



## PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NO.	NAME		
1	GU1	O	External high-side N-channel MOSFET gate drive for the buck regulator BUCK 1. The output provides high peak currents to drive capacitive loads. The gate drive is referred to a floating ground reference provided by the PH1 and has a voltage swing provided by BOOT1
2	PH1	O	Switching terminal of the buck regulator BUCK 1, providing a floating ground reference for the high-side MOSFET gate driver circuitry and is used to sense current reversal in the inductor when discontinuous mode operation is desired.
3	GL1	O	External low-side N-channel MOSFET gate drive for the buck regulator BUCK 1. The output provides high peak currents to drive capacitive loads. The voltage swing on this pin is provided by VREG.
4	PGND1	O	Power ground connection for GL1 driver. Connect to the source of the low-side N-channel MOSFET of BUCK 1.
5	S2	I	High Impedance differential voltage inputs from the current sense element (sense resistor or inductor DCR) for buck controller. For details, see section Functional Description.
6	S1	I	
7	VSENSE1	I	Feedback voltage pin for BUCK1 . For details, see Application Information.
8	COMP1	O	Error amplifier output of BUCK 1 and compensation node for voltage loop stability. The voltage at this node sets the target for the peak current through the respective inductor. This voltage is clamped on the upper and lower ends to provide current limit protection for the external MOSFETs.
9	RST1	O	Open drain power good output for BUCK 1 with a 50kΩ pull-up resistor to S2. An internal power good comparator monitors the voltage at the feedback pin and pull this output low when the output voltage falls by $RSTx_{th1}$ of the set value.
10	SS1	O	Soft-start or tracking input for the buck controller BUCK 1. The buck controller regulates the VSENSE1 voltage to the lower of 0.8V or the SS1 pin voltage. An internal pull-up current source of 1μA is present at the pin and an appropriate capacitor connected here can be used to set the soft-start ramp duration. A resistor divider from another supply can also be used to provide a tracking input to this pin.
11	VSUP	I	Power supply for BUCK3 regulator. Provide good decoupling to PGND3 with ceramic capacitor close to pins.

**PIN FUNCTIONS (continued)**

PIN		I/O	DESCRIPTION
NO.	NAME		
12	PGND3	O	BUCK3 power ground
13	PH3	O	Switching terminal of buck converter BUCK 3. Also provides a floating ground reference for the high-side MOSFET gate driver circuitry .
14	BOOT3	I	A capacitor between BOOT3 and PH3 acts as the voltage supply for the high-side N-channel MOSFET gate drive circuitry in the buck converter BUCK 3. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to re-charge.
15	SS3	O	Soft-start or tracking input for the buck converter BUCK 3. The buck converter regulates the VSENSE3 voltage to the lower of 0.8V or the SS3 pin voltage. An internal pull-up current source of 1µA is present at the pin and an appropriate capacitor connected here can be used to set the soft-start ramp duration. A resistor divider connected to another supply can also be used to provide a tracking input to this pin
16	RST3	O	Open drain power good output for BUCK 3. An internal power good comparator monitors the voltage at the feedback pin and pull this output low when the output voltage falls by RST <sub>xth1</sub> of the set value
17	VSENSE3	I	Feedback voltage pin for BUCK 3. The buck controller regulates the feedback voltage to the internal reference of 0.8V. A suitable resistor divider network between the buck output and the feedback pin sets the desired output voltage
18	COMP3	O	Error amplifier output of BUCK 3 and compensation node for voltage loop stability. The voltage at this node sets the target for the peak current through the respective inductor.
19	SLEW	I	Slew rate (dv/dt) selector of the internal high side switching MOSFET for BUCK3. For details, see Application Information.
20	EN3	I	Enable input for BUCK 3. This input has an internal pull up with approximately 0.5µA current.
21	EN2	I	Enable inputs for BUCK 2. This input has an internal pull up with approximately 0.5µA current.
22	EN1	I	Enable inputs for BUCK 1. This input has an internal pull up with approximately 0.5µA current.
23	SYNC	I	PLL synchronization, low power mode and spread spectrum (TPS43341) control pin. If an external clock is present on this pin the device detects it and the internal PLL locks on to the external clock. This overrides the internal oscillator frequency. The device can synchronize to frequencies from 150 kHz to 600 kHz. For details, see Application Information.
24	Rdelay	O	The capacitor at the Rdelay pin sets the power good delay interval used to de-glitch the outputs of the power good comparators. When this pin is left open, the power good delay is set to an internal default value of 20µs typical.
25	RT	O	The operating switching frequency of the buck controllers and converter is set by connecting a resistor to analog ground on this pin. Shorting this pin to ground defaults operation to 400 kHz for the buck controllers and the converter.
26	GND	O	Analog Ground Reference
27	SS2	O	Soft-start or tracking input for the buck converter BUCK 2. The buck controller regulates the VSENSE2 voltage to the lower of 0.8V or the SS2 pin voltage. An internal pull-up current source of 1µA is present at the pin and an appropriate capacitor connected here can be used to set the soft-start ramp interval. A resistor divider connected to another supply can also be used to provide a tracking input to this pin
28	RST2	O	Open drain power good output for BUCK 2 with a 50kΩ pull-up resistor to S4. An internal power good comparator monitors the voltage at the feedback pin and pull this output low when the output voltage falls by RST <sub>xth1</sub> of the set value
29	COMP2	O	Error amplifier output of BUCK 2 and compensation node for voltage loop stability. The voltage at this node sets the target for the peak current through the respective inductor. This voltage is clamped on the upper and lower ends to provide current limit protection for the external MOSFETs
30	VSENSE2	I	Feedback voltage pin for BUCK 2. The buck controller regulates the feedback voltage to the internal reference of 0.8V. A suitable resistor divider network between the buck output and the feedback pin sets the desired output voltage.
31	S3	I	High Impedance differential voltage inputs from the current sense element (sense resistor or inductor DCR) for buck controller BUCK2. For Details, see section Functional Description.
32	S4	I	
33	PGND2	O	Power ground connection to the source of the low-side N-channel MOSFETs of BUCK 2
34	GL2	O	External low-side N-channel MOSFET for the buck regulator BUCK 2 can be driven from this output. The output provides high peak currents to drive capacitive loads. The voltage swing on this pin is provided by VREG
35	PH2	O	Switching terminal of the buck regulator BUCK 2, providing a floating ground reference for the high-side MOSFET gate driver circuitry and is used to sense current reversal in the inductor when discontinuous mode operation is desired.

**PIN FUNCTIONS (continued)**

PIN		I/O	DESCRIPTION
NO.	NAME		
36	GU2	O	External high-side N-channel MOSFET for the buck regulator BUCK 2 can be driven from this output. The output provides high peak currents to drive capacitive loads. The gate drive is referred to a floating ground reference provided by the PH2 and has a voltage swing provided by BOOT2.
37	BOOT2	I	A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate drive circuitry in the buck converter BUCK 2. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to re-charge.
38	VREG	O	An external capacitor on this pin is required to provide a regulated supply for the gate drivers of the buck controllers and converter. The regulator can be used such that it is either powered from VIN or EXTSUP. This pin has a current limit protection and should not be used to drive any other loads.
39	GPULL	O	Gate driver output to implement the reverse-battery protection by an external PMOS. See Application Information for more details.
40	EXTSUP	I	EXTSUP can be used to supply the VREG regulator from one of the TPS43340/1 buck regulator rails to reduce power dissipation in cases where VIN is expected to be high. When EXTSUP is open or lower than 4.6V, the regulator is powered from VIN.
41	VIN	I	Main Input pin. This is the buck controller and buck converter input pin. Additionally it powers the internal control circuits of the device. A bypass capacitor should be connected to filter noise between this pin and signal ground.
42	VLR1	I	The VLR1 terminal is the input voltage source for the linear regulator supply. An input capacitor to ground is required to filter any noise present on the line.
43	VIN2SENSE	I	Supply voltage sense input for current mode of BUCK2. The is required when BUCK2 is used in a cascade configuration. This configuration does not support LPM on Buck2.
44	RST4	O	Open drain power good indicator pin for LREG1 with a 50kΩ pull-up resistor to LREG1. An internal power good comparator monitors the voltage at the feedback pin and pull this output low when the output voltage falls by $RSTx_{th1}$ of the set value
45	VSENSE4	I	Feedback voltage pin for Linear regulator LREG1. LREG1 regulates the feedback voltage to the internal reference. A suitable resistor divider network between the LDO output and the feedback pin sets the desired output voltage. See LREG1 parameters above and Application Information.
46	LREG1	O	Linear regulator output. Decouple with a low ESR ceramic output capacitor connected from this terminal to ground.
47	EN4	I	Enable input for LREG1 (active high with an internal pull up current source). An input voltage higher than $V_{ih}$ enables the regulator, while an input voltage lower than $V_{il}$ disables the regulator. This input has an internal pull up with approximately 0.5μA current.
48	BOOT1	I	A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate drive circuitry in the buck converter BUCK 1. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to re-charge.

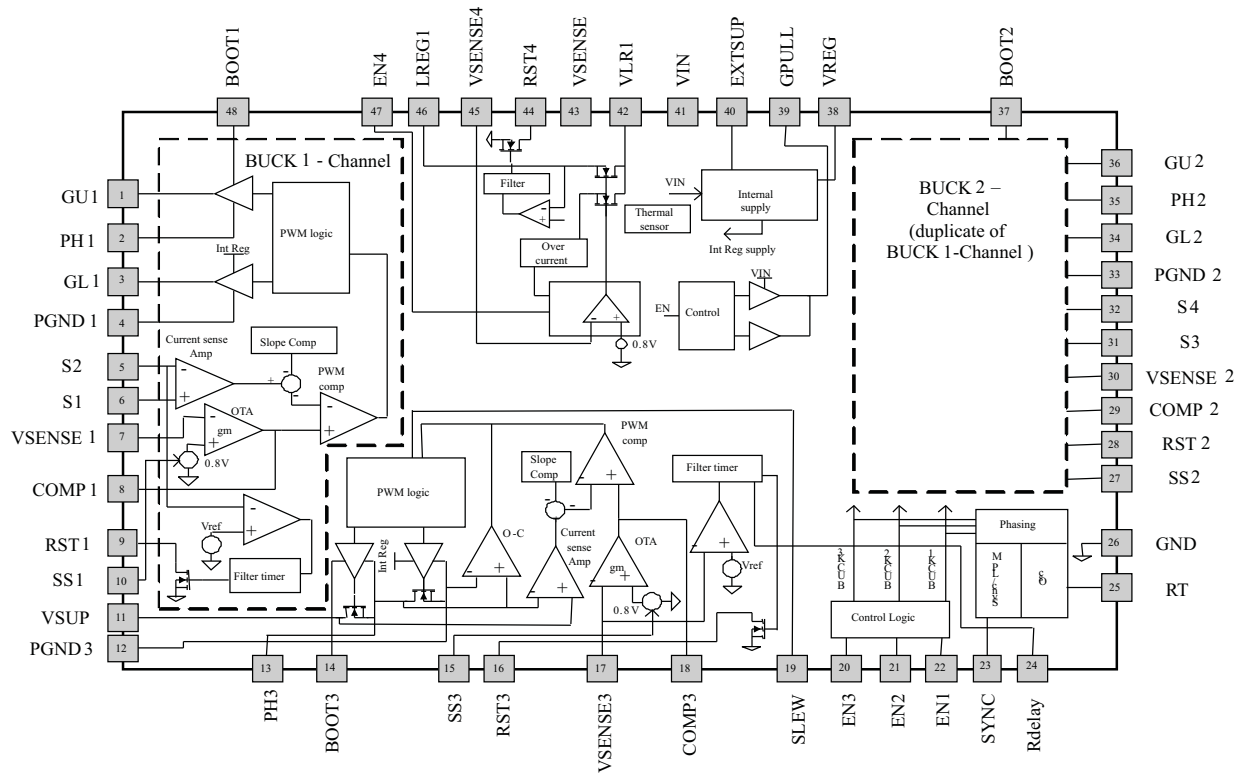


Figure 2. Internal Functional Blocks

## FUNCTIONAL DESCRIPTION

### Enable Inputs

All regulators are enabled using independent enable inputs at the EN1.. EN4 pins. These pins have internal pull-up currents of 0.5  $\mu$ A (typical). As a result, an open circuit on these pins enables the respective regulators. EN1, EN2, EN4 are high voltage pins and can be connected directly to the battery for self-bias. When all regulators are disabled, the device is shut down and consumes a current of 5  $\mu$ A typical.

### BUCK CONTROLLERS: NORMAL MODE PWM OPERATION

#### Setting the Operating Frequency

The buck controllers operate using constant frequency peak current mode control for optimal transient behavior and ease of component choices. The switching frequency is programmable between 150 kHz and 600 kHz depending upon the resistor value at the RT pin. Tying this pin to ground at this pin sets the default switching frequency to 400 kHz. The frequency can also be set by a resistor at RT according to the formula

$$f_{sw} = 24 \times 10^9 / RT \quad (1)$$

#### Switching Frequency

For example,

600 kHz requires 40 k $\Omega$

150 kHz requires 160 k $\Omega$

It is also possible to synchronize to an external clock at the SYNC pin in the same frequency range of 150 kHz to 600 kHz. The device detects clock pulses at this pin and an internal PLL locks on to the external clock within the specified range. The device can also detect a loss of clock at this pin and when this is detected for  $f_{SW-Trans-delay}$  it sets the switching frequency to the internal oscillator. The two buck controllers operate at the same switching frequency 180 degrees out of phase.

#### Feedback Inputs

The output voltages are set by choosing the right resistor feedback divider networks connected to the VSENSE<sub>x</sub> (feedback) pins. This is to be chosen such that the regulated voltages at the VSENSE<sub>x</sub> pins equals 0.8V. The VSENSE<sub>x</sub> pins have 100nA pull up current sources as a protection feature in case the pins open up as a result of physical damage.

$$V_{BUCKx} = 0.8 \left( 1 + \frac{R_{TOP}}{R_{BOTTOM}} \right) V \quad (2)$$

#### Output Voltage

Where,  $R_{TOP}$  is the resistor from VBUCK<sub>x</sub> to VSENSE<sub>x</sub> and  $R_{BOTTOM}$  is the resistor from VSENSE<sub>x</sub> to ground

#### Soft-Start Inputs

In order to avoid large inrush currents, both buck controllers have independent programmable soft-start timing. The voltage at the SS<sub>x</sub> pins acts as the soft-start reference voltage. A 1  $\mu$ A pull-up current is available at the SS<sub>x</sub> pins and by choosing a suitable capacitor a desired soft-start ramp speed can be generated. After start-up, the pull-up current ensures that pins SS<sub>x</sub> are higher than the internal reference of 0.8V which then becomes the reference for the buck controllers. The required capacitor for  $\Delta t$ , the desired soft-start time is given by:

$$C_{SS} = \frac{I_{SS} \times \Delta t}{\Delta V} \quad (3)$$

#### Soft Start Ramp Capacitor

where:

$I_{SS} = 1 \mu$ A (typical)

$\Delta V = 0.8$  V

Alternatively the soft-start pins can be used as tracking inputs. In this case, the pins should be connected to the supply to be tracked via a suitable resistor divider network.

## Current Mode Operation

Peak current-mode control regulates the peak current through the inductor such that the output voltage is maintained to its set value. The error between the feedback voltage at VSENSE<sub>x</sub> and the internal reference produces a signal at the output of the error amplifier (COMP<sub>x</sub>) which serves as target for the peak inductor current. The current through the inductor is sensed as a differential voltage at S1-S2/S3-S4 and compared with this target during each cycle. A fall or rise in load current produces a rise or fall in voltage at VSENSE<sub>x</sub> causing COMP<sub>x</sub> to fall or rise respectively, thus increasing/decreasing the current through the inductor until the average current matches the load. In this way the output voltage is maintained in regulation.

The High-Side N-channel MOSFET is turned on at the beginning of each clock cycle and kept on until the inductor current reaches its peak value. Once this MOSFET is turned off, and after a small delay (shoot-through delay) the lower N-channel MOSFET is turned on until the start of the next clock cycle. In dropout operation the high-side MOSFET stays on 100%. In every fourth clock cycle the duty cycle is limited to 95% in order to charge the bootstrap capacitor at BOOT<sub>x</sub>. This allows a maximum duty cycle of 98.75% for the buck regulators. Thus during dropout the buck regulators switch at one-fourth of the normal frequency.

## Current Sensing and Current Limit with Foldback

The maximum value of COMP<sub>x</sub> is clamped such that the maximum current through the inductor is limited to a specified value. When the output of the buck regulator (and hence the feedback value at VSENSE<sub>x</sub>) falls to a low value due to a short circuit/over-current condition, the clamping voltage at the COMP<sub>x</sub> successively decreases, thus providing current fold back protection. This protects the high-side external MOSFET from excess current (forward direction current limit).

Similarly, if due to a fault condition the output is shorted to a high voltage and the low-side MOSFET turns fully on, the COMP<sub>x</sub> node will drop low. It is clamped on the lower end as well in order to limit the maximum current in the low-side MOSFET (reverse direction current limit).

The current through the inductor is sensed by an external resistor. The sense resistor should be chosen such that the maximum forward peak current in the inductor generates a voltage of 75 mV across the sense pins. This value is specified at low duty cycles only. At typical duty cycle conditions around 40% (assuming 5 V output and 12V input), 50 mV is a more reasonable value, considering the slope compensation and tolerances. The typical characteristics in Figure 18 provide a guide for using the correct current limit sense voltage.

The current sense pins S<sub>x</sub> are high impedance pins with low leakage across the entire output range. This allows DCR current sensing using the DC resistance of the inductor for higher efficiency. DCR sensing is shown in the below figure. Here the series resistance (DCR) of the inductor is used as the sense element. The filter components should be placed close to the device for noise immunity. It should be remembered that while the DCR sensing gives high efficiency, it is less accurate due to the temperature sensitivity and a wide variation of the parasitic inductor series resistance. Hence it may often be advantageous to use the more accurate sense resistor for current sensing.

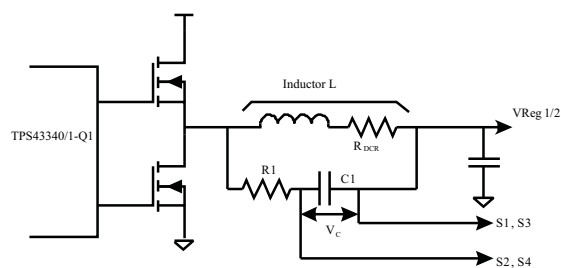


Figure 3. DCR Sensing Configuration

## Slope Compensation

Optimal slope compensation which is adaptive to changes in input voltage and duty cycle allows stable current mode operation at all conditions. For optimal performance of this circuit, the following condition must be satisfied in the choice of inductor and sense resistor:

$$L = \frac{200}{f_{sw}} \times R_s \quad (4)$$

### Inductor and Sense Resistor Choice

Where

L is the buck regulator inductor in Henry

R<sub>S</sub> is the sense resistor in Ω

f<sub>sw</sub> is the buck regulator switching frequency in Hz

## Reset Outputs and Filter Delays

Each buck controller has an independent reset comparator monitoring the feedback voltage at the VSENSEx pins and indicating whether the output voltage has fallen below the specified reset threshold. The reset indicator is available as an open drain output at the RSTx pins. An internal 50 kΩ pull-up resistor to S2/S4 is available or an external resistor can be used. When a buck controller is shut down, the power good outputs are pulled down internally. Connecting the pull-up resistor to a rail other than the output of that particular buck channel will cause a constant current flow through the resistor when the buck controller is powered down.

In order to avoid triggering the power good indicators due to noise or fast transients on the output voltage, an internal delay of t<sub>deglitch</sub> for de-glitching is used. When the output voltage reaches its set value after a start-up ramp or negative transient, the power good indicator will be asserted high (the open-drain pin released) after a delay of t<sub>delay</sub>, at least t<sub>delay\_fix</sub>. This can be used to delay the reset to the circuits being powered from the buck regulator rail. The delay of this circuit can be programmed by using a suitable capacitor at the Rdelay pin according to [Equation 5](#):

### Power Good Output Delay

$$t_{Rdelay} = 10^6 \times C_{Rdelay} \text{ (seconds)} \quad (5)$$

Where

C<sub>Rdelay</sub> is the capacitor value in Farad on Rdelay pin.

When the Rdelay pin is open the delay is set to a default value of 20 μs typical. The power good delay timing is common to all supply rails but the power good comparators and outputs function independently.

## Light Load PFM Mode

An external clock or a high level on the SYNC pin or enabling BUCK3 results in forced continuous mode operation of the bucks. When the SYNC pin is low or open, the buck controllers will be allowed to operate in discontinuous mode at light loads by turning off the low-side MOSFET whenever a zero-crossing in the inductor current is detected.

In discontinuous mode, as the load decreases, the duration of the clock period when both the high-side as well the low-side MOSFET is turned off increases (deep discontinuous mode). In case the duration exceeds 60% of the clock period and VBAT >8V, the buck controller switches to a low power operation mode. The design ensures that this typically occurs at 1% of the set full load current if the inductor and the sense resistor have been chosen appropriately as recommended in the slope compensation section.

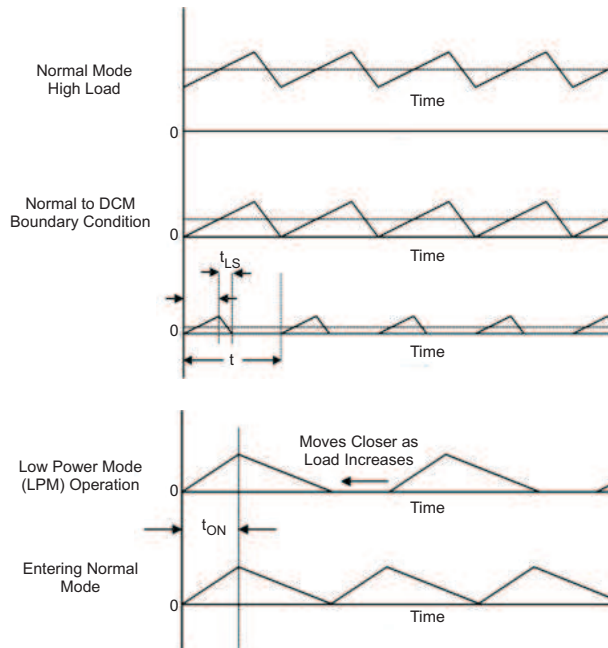


Figure 4.

In Low Power PFM Mode, the buck controllers monitor the VSENSEx voltage and compare it with the 0.8 V internal reference. Whenever the VSENSEx value falls below the reference, the high-side MOSFET is turned on for a pulse-duration inversely proportional to the difference  $V_{IN}-S_2/S_4$ . At the end of this on-time, the high-side MOSFET is turned off and the current in the inductor decays until it becomes zero. The low-side MOSFET is not turned on. The next pulse occurs the next time VSENSEx falls below the reference value. This results in a constant volt-second  $T_{ON}$  hysteretic operation with a total device quiescent current consumption of 30  $\mu A$  when a single buck channel is active and 35  $\mu A$  when both channels are active.

As the load increases, the pulse become more and more frequent until the current in the inductor becomes continuous. At this point, the buck controller returns to normal fixed frequency current mode control. Another criterion to exit the low power mode is when  $V_{IN}$  falls low enough to require higher than 80% duty cycle of the high-side MOSFET.

The TPS43340/1-Q1 can support the full current load during low power mode until the transition to normal mode takes place. The design ensures the low power mode exit occurs at 10% (typical) of full load current if the inductor and sense resistor have been chosen as recommended. Moreover, there is always a hysteresis between the entry and exit thresholds to avoid oscillating between the two modes.

In the event that both buck controllers are active, low power mode is only possible when both buck controllers have light loads that are low enough for low power mode entry.

### Frequency-Hopping Spread Spectrum (TPS43341-Q1 Only)

The TPS43341-Q1 features a frequency-hopping pseudo-random spectrum spreading architecture. On this device, whenever the SYNC pin is high, the internal oscillator frequency is varied from one cycle to the next within a band of  $\pm 5\%$  around the value programmed by the resistor at the RT pin. The implementation uses a linear feedback shift register that changes the frequency of the internal oscillator based on a digital code. The shift register is long enough to make the hops pseudo-random in nature and is designed in such a way that the frequency shifts only by one step at each cycle to avoid large jumps in the switching frequencies.

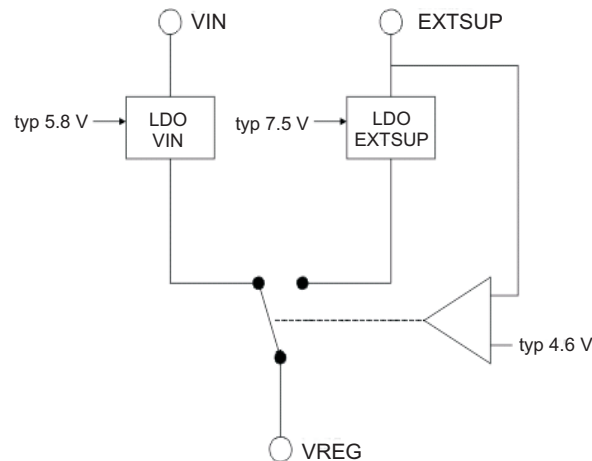
**Table 1. Frequency Hopping Control**

SYNC TERMINAL	FREQUENCY SPREAD SPECTRUM (FSS)	COMMENTS
External clock	Not active	Buck controllers in forced continuous mode (CCM), internal PLL locks into external clock between 150 kHz and 600 kHz
Low or open	Not active	Device can enter discontinuous mode. Automatic LPM entry and exit depending on load conditions.
High	TPS43340-Q1: FSS active	Buck controllers operates in forced continuous mode (CCM)
	TPS43341-Q1: FSS not active	Buck controllers operate in forced continuous mode (CCM)

### Gate Driver Supply (VREG, EXTSUP)

The gate drivers of the buck controllers and the buck converter are supplied from an internal linear regulator whose output (5.8 V typical) is available at the VREG pin and should be decoupled using at least a 3.3  $\mu$ F ceramic capacitor. This pin has an internal current limit protection and should not be used to power any other circuits.

The VREG linear regulator is powered from VIN by default when the EXTSUP voltage is lower than 4.6 V (typical). If VIN is expected to go to high levels, there can be excessive power dissipation in this regulator, especially at high switching frequencies and when using large external MOSFET's. In this case, it is advantageous to power this regulator from the EXTSUP pin which can be connected to a supply lower than VIN but high enough to provide the gate drive. When EXTSUP is connected to a voltage greater than 4.6 V, the linear regulator automatically switches to EXTSUP. Efficiency improvements are thus possible when one of the switching regulator rails from the TPS43340/1-Q1 or any other voltage available in the system is used to power the EXTSUP.



**Figure 5. Internal Gate Driver Supply**

Using a large value for EXTSUP is advantageous as it provides a large gate drive and hence better on-resistance of the external MOSFETs. The EXTSUP pin should be tied to ground when not being used.

During low power mode, the EXTSUP functionality is not available. The internal regulator operates as a shunt regulator powered from VIN and has a typical value of 7.2 V. Current limit protection for VREG is available in low power mode as well.

### External P-Channel Drive (GPULL) and Reverse Battery Protection

The TPS43340/1-Q1 includes a gate driver for an external P-channel MOSFET which can be used for reverse battery protection. This is useful to reduce the voltage drop across the protection element compared to using a series diode to VIN. The gate – source voltage of the external PMOS is clamped by an internal Zener diode to 17 V typical.

$V_{BAT} = V_F \rightarrow |V_{GS}| = 0\text{ V} \rightarrow \text{FET and Diode NOT conducting}$   
 $V_F = V_{BAT} = V_T (\text{FET}) \rightarrow |V_{GS}| = V_{BAT} \rightarrow \text{FET NOT conducting and Diode conducting}$   
 $V_T (\text{FET}) = V_{BAT} = 17\text{ V} \rightarrow |V_{GS}| = V_{BAT} \rightarrow \text{FET conducting}$   
 $V_{BAT} = 17\text{ V} \rightarrow |V_{GS}| = 17\text{ V} \rightarrow \text{FET conducting}$

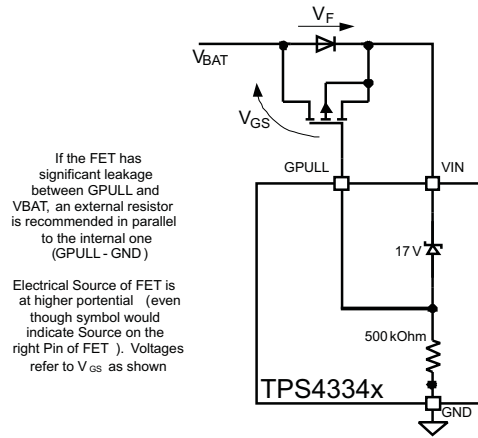


Figure 6. Internal Circuit of GPULL Output

### Undervoltage Lockout and Overvoltage Protection

The TPS43340/1-Q1 will start up at a VIN voltage of 6.5 V (max). Once it has started up, the device operates down to a VIN undervoltage lockout level of 3.6 V or until VREG undervoltage of 3.6V is reached. A voltage above 46 V at VIN shuts down the device. In order to prevent transient spikes from shutting down the device, the under and overvoltage protection have filter times of 5  $\mu\text{s}$  (typical). Overvoltage protection is not supported in LPM.

When the voltages return to the normal operating region, the enabled regulators start including new soft-start ramps.

### Thermal Protection

The TPS43340/1-Q1 is protected from over-temperature using an internal thermal shutdown circuit. If the die temperature exceeds the thermal shutdown threshold (e.g. due to fault conditions such as a short circuit at the gate drivers or VREG), the device is turned off and restarted when the temperature has fallen by the hysteresis.

Table 2. Low Power Mode Operation of the System

SETUP	SYNC	QUIESCENT CURRENT (TYP), NO LOAD, 25°C	DESCRIPTION
BUCK1 or BUCK2 in LPM mode	Low	~30 $\mu\text{A}$	Configuration for Ignition off applications with standby functionality
BUCK1 and BUCK2 in LPM mode		~35 $\mu\text{A}$	
BUCK1 or BUCK2 in PWM mode	High	~30-40 mA	Including switching currents
BUCK1 and BUCK2 in PWM mode		~30-40 mA	Including switching currents
LREG1	N/A	~50 $\mu\text{A}$	Configuration for Ignition off applications with standby functionality
LREG1 and BUCK1 or 2 in LPM mode	Low	~55 $\mu\text{A}$	
LREG1 and BUCK1 and 2 in LPM mode		~60 $\mu\text{A}$	
LREG1 and BUCK1 or 2 in PWM mode	High	30-40 mA	Including switching currents
LREG1 and BUCK1 and 2 in PWM mode		30-40 mA	Including switching currents

The synchronous Buck Converter VBUCK3 with the integrated FETs does not support LPM. If VBUCK3 is turned on the system will be forced to operate in normal mode and the quiescent current consumption will increase.

**Table 3. Input Voltage and Low Power Mode Operation**

INPUT VOLTAGE AT VIN PIN	LOAD CURRENT OF LREG1	CHARGE PUMP OF LREG1	BUCK CONTROLLER VBUCK1 AND VBUCK2	VIN QUIESCENT CURRENT (TYP), NO LOAD, 25°C	DESCRIPTION
VIN > 9 V	N/A	OFF	LPM allowed	55 µA	Lowest current consumption of the system at VIN (LREG1, VBUCK1&2 enabled), typ. ignition off stay alive mode with up to 3 voltage rails active
7.5 V < VIN < 9 V	< 2mA	OFF	LPM allowed	55 µA	
	> 6mA	ON	LPM allowed	260 µA	
VIN < 7.5 V	N/A	ON	LPM not allowed	2.6 mA	If VIN drops below 7.5 V, the Buck Controllers VBUCK1&2 will leave Low Power Mode (LPM) and start PWM operation, quiescent current of the system will increase. For applications that use the LREG1 only as standby keep alive supply, quiescent current is still low.

The threshold for the charge pump of the low quiescent linear regulator LREG1 to be turned on is monitored at the VIN pin. If LREG1 is used as post regulator with an input voltage VLR1 of less than 7.5 V, the charge pump will still stay off as long as the required conditions for VIN and the load current are met. The sampling interval for the above voltage thresholds at the VIN pin is typically 60 µs.

### Phase Configuration

The IC is configured with Buck controller 1 and Buck controller switching 180 degrees out of phase. Buck converter (Buck 3) switches in phase with Buck controller 1.

CONFIGURATION	VBUCK1	VBUCK2	VBUCK3	DESCRIPTION
Phase	0 deg	180 deg	0 deg	VBUCK1 and 2 out of phase, VBUCK 1 and 3 in phase

### SYNCHRONOUS BUCK CONVERTER BUCK3

This regulator operates with the switching frequency set on the RT terminal or an external clock input on SYNC terminal. The internal power FETs are switched out of phase to regulate the output voltage operating in a pulse width modulation. The converter utilizes a peak current mode control loop with external frequency compensation. The synchronous operation mode improves the overall efficiency.

### Softstart and Foldback Functions

The converter soft start is set by a capacitor on the SS3 terminal and is activated when the enable pin on EN3 is pulled high. During soft start or whenever the voltage on VSENSE3 falls below limits given by  $f_{SW-f-back}$  the converter will switch to frequency foldback of  $f_{sw}/2$  to help control the coil current. In addition to the frequency foldback, the converter is protected against output short to ground by implementation of current fold back to reduce power dissipation. Like in the BUCK controllers, the current foldback reduces the maximum peak current limit depending on the voltage on the VSENSE3 pin. The characteristic of the current foldback is shown in Figure 15.

### Current Mode Control and Current Limit Protection

The coil peak current is measured using the high side integrated FET and is regulated in each switching cycle in accordance to the voltage on the COMP3 pin. Similarly to BUCK controllers 1 and 2, COMP3 is an output of an transconductance error amplifier of the voltage feedback loop and sets the target for the peak current comparator (inner current loop). COMP3 is used for frequency compensation of the voltage loop utilizing a type II compensation network.

By clamping the voltage on the COMP3 node, the positive current limit is realized. The positive clamping level depends on the voltage on the VSENSE3 pin, as described above. Clamping is also implemented for low voltage on the COMP3 pin, which speeds up the transient response after output overshoot. The current limit set by COMP3 is adjusted during the switching cycle by the internal slope compensation for stability of the current loop.

For correct operation of the slope compensation, the coil used for BUCK3 must satisfy the following:

$$L_{\text{BUCK3}} = 3.7/f_{\text{sw}} \quad (6)$$

Where:

- $L_{\text{BUCK3}}$  is the inductance in Henry
- $f_{\text{sw}}$  is the switching frequency in Hz

When the positive current limit is reached during the high PWM phase, PWM is reset. The high side FET is turned off and the low part of the cycle is initiated. If an overcurrent condition is detected during the PWM low phase, such as during an output short to a supply, the lowside FET is turned off till the end of the given cycle, to allow the coil current to flow through the body diode of the high side FET.

### Operation in Dropout and Undervoltage Protection

This converter is capable of operating with low input to output voltage difference. In dropout operation the integrated high-side MOSFET stays on 100%. In every fourth clock cycle the duty cycle is limited to 95% in order to charge the bootstrap capacitor at BOOT3. This allows a maximum duty cycle of 98.75% for the buck converter. In this mode the output will track the input until the internal under voltage lock out is initiated due to low supply voltage on the VSUP pin.

Thermal shutdown monitors the virtual junction temperature of the integrated FETs. When  $T_j = 170^\circ\text{C}$  is exceeded, both the high and low side switches are turned off. The converter will return to normal operation when the temperature decreases to the acceptable level (typically  $T_j = 150^\circ\text{C}$ )

### Slew Rate Control (SLEW)

The slew for BUCK3 is set by digital setting on this terminal. Setting the slew rate to logic high (slowest slew rate) extends the minimum on time of the BUCK converter by 5% of the clock period.

SLEW TERMINAL SETTING	$t_r$ (TYP) ns	$t_f$ (TYP) ns
Slew > VREG – 0.2 V (low slew rate, logic high)	24	7
Slew pin open – medium slew rate	11	3
Slew < 0.2 V (fast slew rate, logic low)	8	2

### LINEAR REGULATOR (LREG1)

The linear regulator is an NMOS output low drop out regulator with output load current up to 300mA. It can be operated directly from the battery. When EN4 is tied high or open, LREG1 will turn on its output following an internally generated softstart ramp. The regulation loop uses internal frequency compensation. If the output is shorted to ground the device will protect by limiting the current. For VIN lower than 9V then LREG1 will control the internal charge pump depending on VIN and the load current in accordance with Table 3. An internal voltage selector selects the higher available supply for the error amplifier between VIN and the charge pump voltage. The output voltage of the low-dropout regulator is monitored for undervoltage and its state is signaled on pin RST4.

TYPICAL CHARACTERISTICS

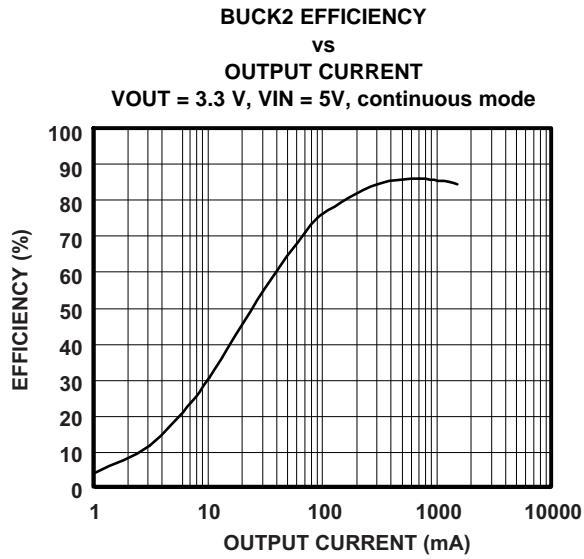


Figure 7.

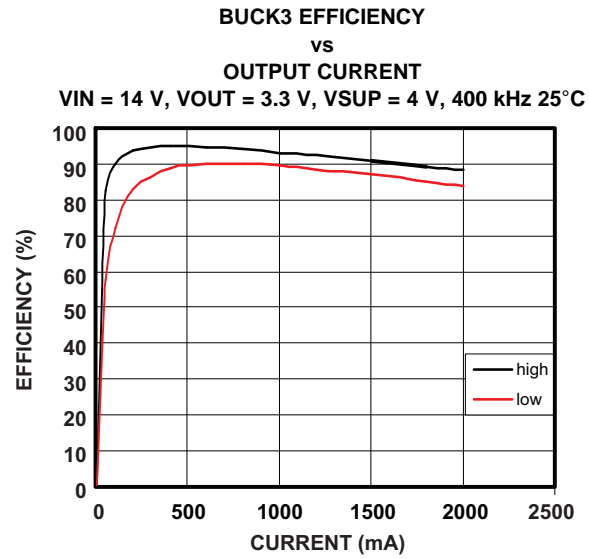


Figure 8.

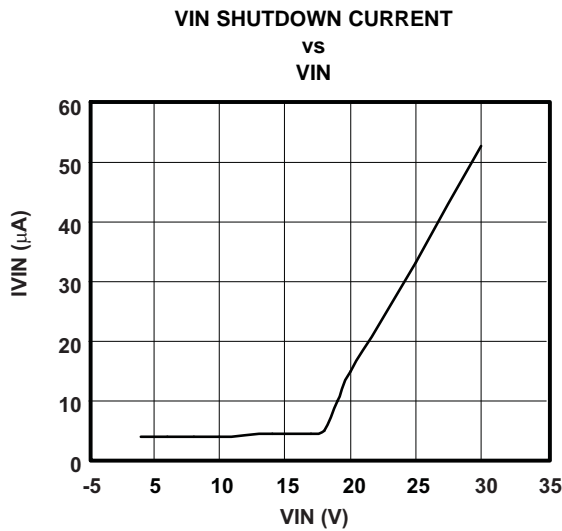


Figure 9.

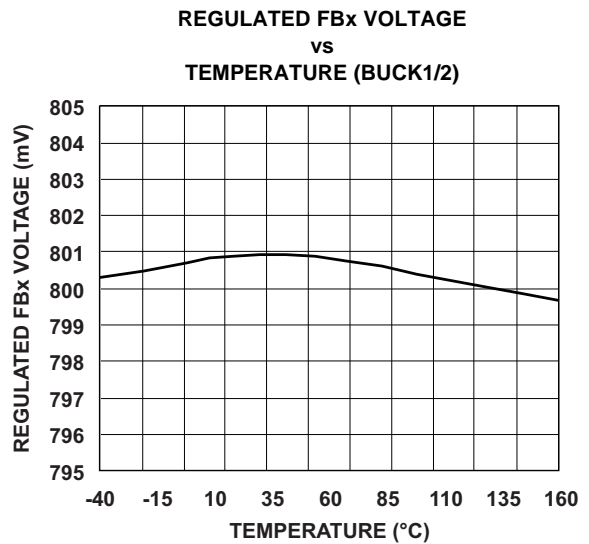


Figure 10.

**TYPICAL CHARACTERISTICS (continued)**

**BUCK1/2 LOAD STEP: LOW POWER MODE ENTRY**  
(0.09 mA TO 4 A AT 2.5 A/μs)

VIN = 12V, VOUT = 5V, SWITCHING FREQUENCY = 400 kHz  
INDUCTOR = 4.7 μH, RSENSE = 10 mΩ

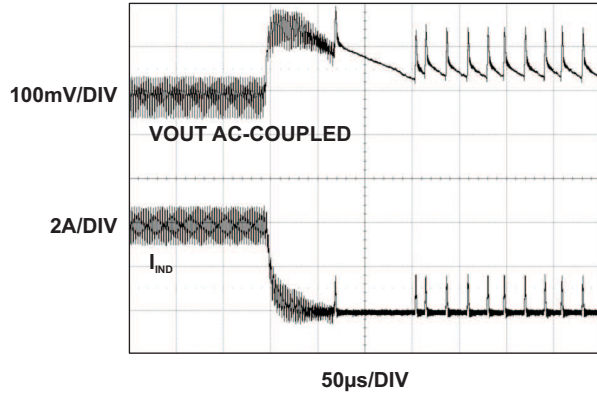


Figure 11.

**BUCK1/2 LOAD STEP: LOW POWER MODE EXIT**  
(0.09 mA TO 4 A AT 2.5 A/μs)

VIN = 12 V, VOUT = 5 V, SWITCHING FREQUENCY = 400 kHz  
INDUCTOR = 4.7 μH, RSENSE = 10 mΩ

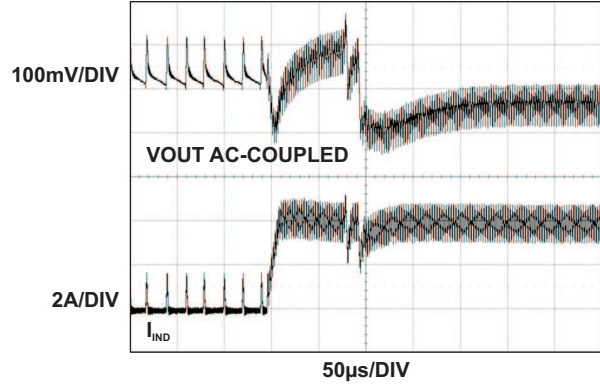


Figure 12.

**INDUCTOR CURRENTS (BUCK1/2)**

VIN = 12 V, VOUT = 5 V, SWITCHING FREQUENCY = 400 kHz  
INDUCTOR = 4.7 μH, RSENSE = 10 mΩ

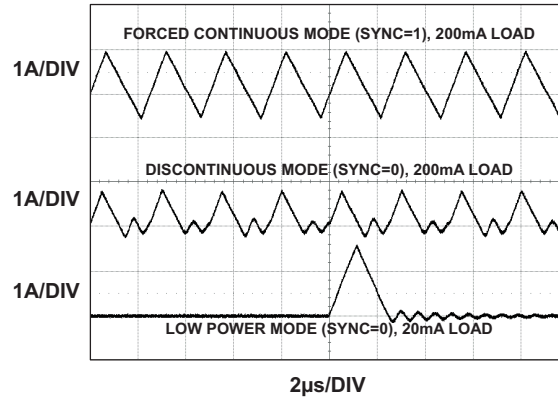


Figure 13.

TYPICAL CHARACTERISTICS (continued)

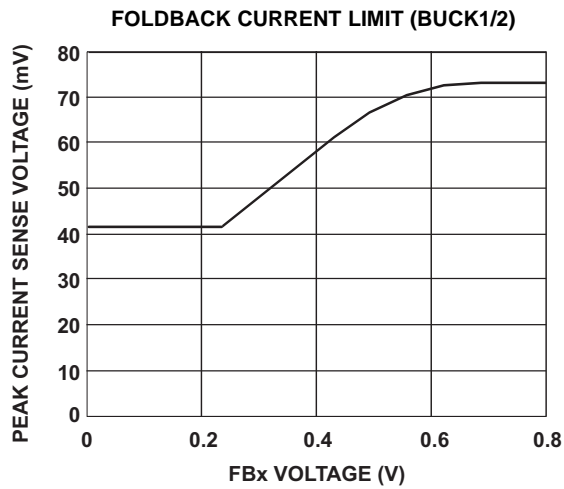


Figure 14.

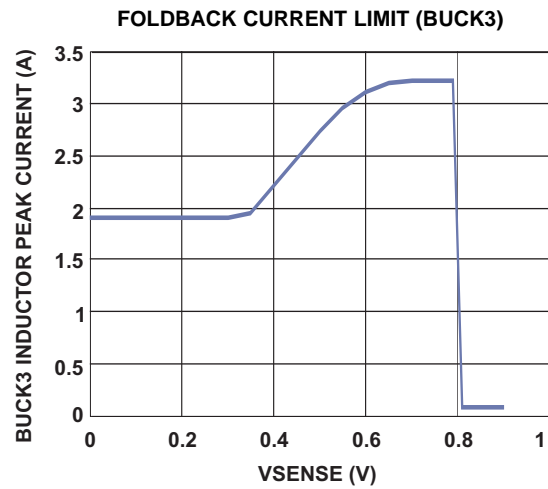


Figure 15.

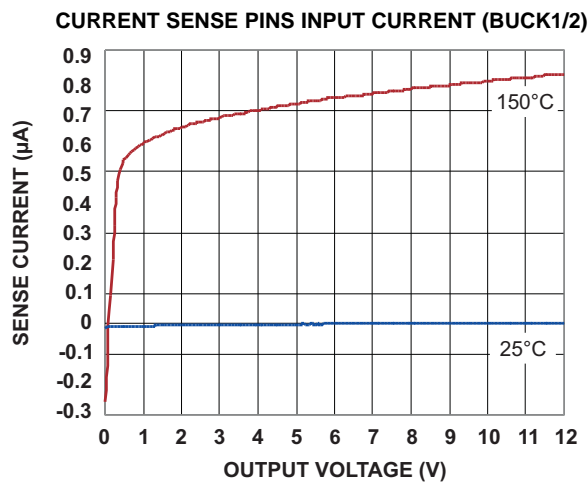


Figure 16.

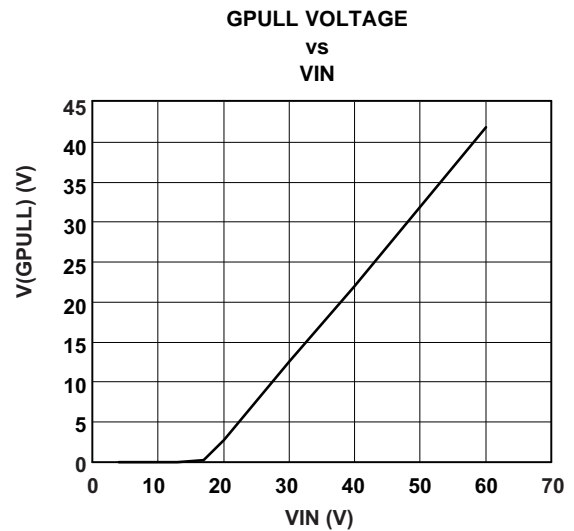


Figure 17.

**TYPICAL CHARACTERISTICS (continued)**

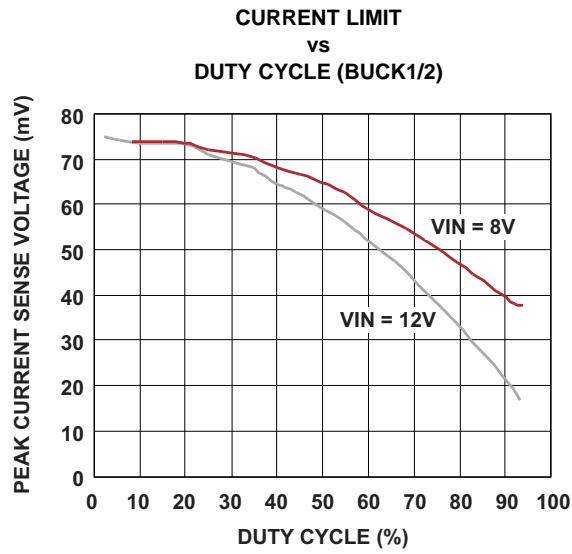


Figure 18.

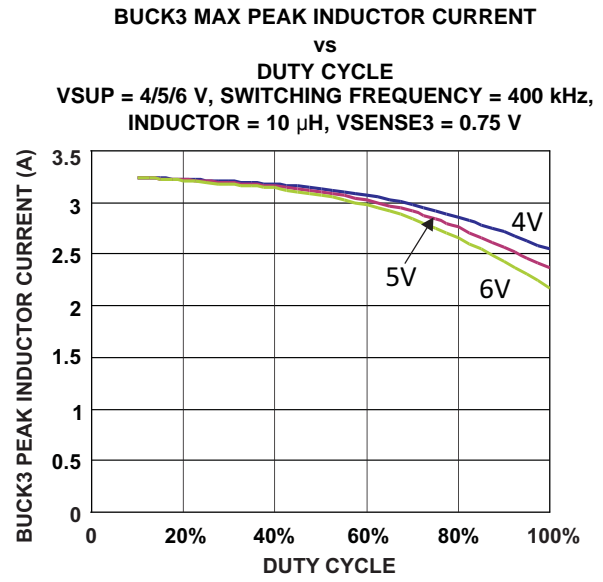


Figure 19.

## APPLICATION INFORMATION

### High- and Low-Side Power NMOS Selection for the BUCK Converters

The gate drive supply for these MOSFET is supplied by an internal supply which is 5.8 V typical under normal operating conditions. The output is a totem pole allowing full voltage drive of VREG to the gate with peak output current of 0.6 A. The high-side MOSFET is referenced to the phase terminal (PHx) and the low-side MOSFET is referenced to power ground (PGNDx) terminal. For a particular applications these MOSFETs should be selected with consideration for the following parameters  $R_{DS(ON)}$ , gate charge  $Q_g$ , drain to source breakdown voltage  $BVDSS$ , Maximum DC current  $I_{DC(max)}$  and thermal resistance for the package.

#### Power dissipation on the High-side FET ( $P_{D\_HS}$ ):

$$(I_O)^2 \times R_{DS(on)}(1 + TC) \times D + \left( \frac{V_I \times I_O}{2} \right) \times (t_r + t_f) \times f_{SW} \quad (7)$$

First term is conduction losses

Second term is switching losses

#### Power dissipation on the Low-side FET ( $P_{D\_LS}$ ):

$$(I_O)^2 \times R_{DS(on)}(1 + TC) \times (1 - D) + V_f \times I_O (t_{dead}) \times f_{SW} \quad (8)$$

First term is conduction losses

Second term is switching losses FET body diode losses during deadtime

NOTE: The  $R_{DS(ON)}$ , has a positive temperature coefficient TC which is typically 0.4%/°C

Gate losses for highside and lowside FETs:

indent (9)

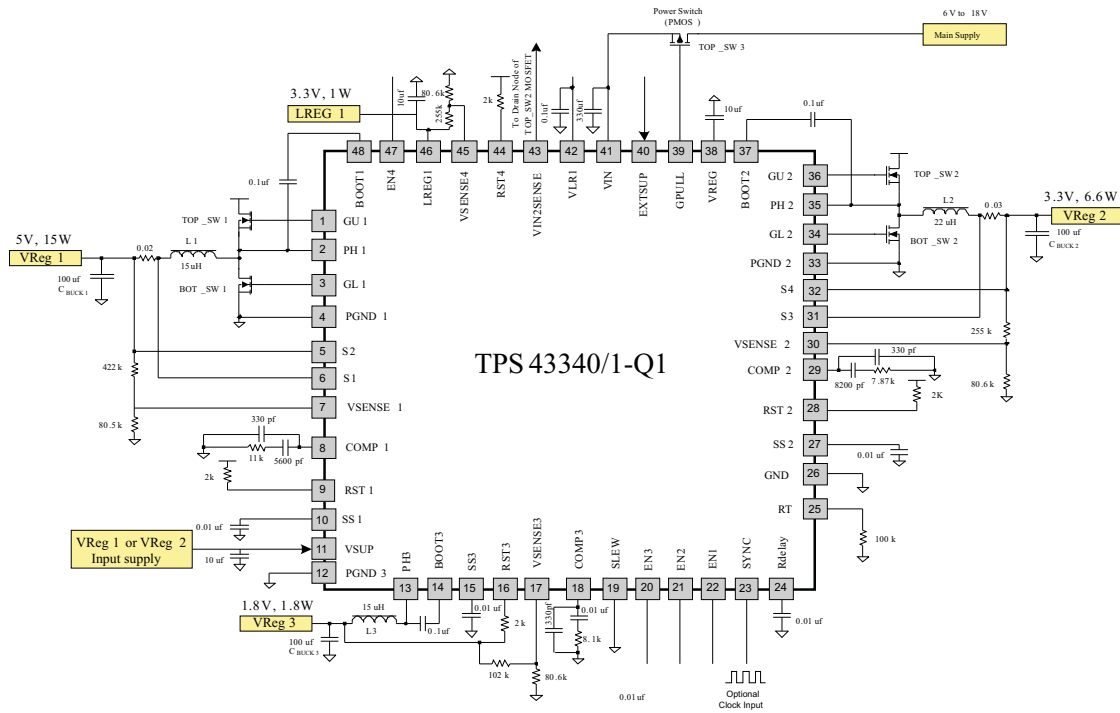
$$P_{BUCK \times GATE} = 2 \times f_{sw} \times Q_g \times V_{VREG} \quad (10)$$

### Design Guide - Step-by-Step Design Procedure

The following example illustrates the design process and component selection for the TPS43340/1-Q1. The design goal parameters are given in [Table 4](#).

**Table 4.**

PARAMETER	BUCK1	BUCK2	BUCK3
Input voltage, $V_I$	6 V to 18 V 14 V - typ	6 V to 18 V 14 V - typ	4 V to 10 V 5 V - typ
Output ripple voltage	±0.2 V	±0.2 V	±0.1 V
Output voltage, $V_O$	5 V ±2%	3.3 V ±2%	1.8 V ±2%
Max - output current, $I_O$	4.5 A	4.5 A	2.2 A
Min - output current, $I_O$	0.1 A	0.1 A	0.1 A
Load step output tolerance, $\Delta V_O$	±0.2 V	±0.2 V	±0.75 V
Current output load step, $\Delta I_O$	0.1 A to 4.5 A	0.1 A to 4.5 A	0.1 A to 2.2 A
Converter switching frequency, $f_{sw}$	400 kHz	400 kHz	400 kHz
Junction Temperature, $T_J$	125°C	125°C	125°C



- L1, L2, L3: DR127-8R2-R (Coiltronics)
- TOP\_SW3: IRF7663TRPBF (International Rectifier)
- TOP\_SW1, BOT\_SW2: Si4946BEY-T1-E3 (Vishay)
- TOP\_SW2, BOT\_SW2: Si4946BEY-T1-E3 (Vishay)
- CBUCK1, CBUCK2, CBUCK3: AVX- TPSD107K016R0060 (AVX)

Figure 20. Application Schematic

### Buck1 Component Selection

#### Duty Cycle

$$D = \frac{5}{14} = 0.357 \tag{11}$$

#### Selection of Current Sensing Resistor

$$R_{SENSE} = \frac{0.075 \text{ V}}{4.5 \text{ A}} = 0.017 \Omega \tag{12}$$

Use 10 mΩ to allow for ripple-current.

#### Inductor Selection L

$$L = 200 \times \frac{0.01 \Omega}{400 \text{ kHz}} = 5 \mu\text{H} \tag{13}$$

Use 8.2 μH.

#### Inductor Ripple Current

$$\Delta I_{L_{RIPPLE}} = \frac{5 \text{ V}}{400 \text{ kHz} \times 8.2 \mu\text{H}} \times \left(1 - \frac{5 \text{ V}}{14 \text{ V}}\right) = 0.98 \text{ A} \tag{14}$$

#### Output Capacitor C<sub>O</sub>

$$C_O = \frac{2 \times 4.5 \text{ A}}{400 \text{ kHz} \times 0.2 \text{ V}} = 112 \mu\text{F} \tag{15}$$

Use 100 μF.

**Input Capacitor C<sub>I</sub>**

$$C_I = \frac{0.25 \times 4.5 \text{ A}}{400 \text{ kHz} \times 0.5 \text{ V}} = 5.6 \mu\text{F} \quad (16)$$

Use 10  $\mu\text{F}$ , shared between Buck1 and Buck2.

**High-Side MOSFET (TOP\_SW1)**

$$(4.5 \text{ A})^2 \times 0.009 \times (1 + 0.4) \times 0.357 + \left( \frac{14 \text{ V} \times 4.5 \text{ A}}{2} \right) \times (20 \text{ ns} + 20 \text{ ns}) \times 400 \text{ kHz} = 0.59 \text{ W} \quad (17)$$

**Low-Side MOSFET (BOT\_SW1)**

$$(4.5 \text{ A})^2 \times 0.009 \times (1 + 0.4) \times 1 - 0.357) + 0.6 \text{ V} \times 4.5 \text{ A} \times (2 \times 20 \text{ ns}) \times 400 \text{ kHz} = 0.21 \text{ W} \quad (18)$$

**Buck2 Component Selection**
**Duty Cycle**

$$D = \frac{3.3}{14} = 0.236 \quad (19)$$

**Selection of Current Sensing Resistor**

$$R_{\text{SENSE}} = \frac{0.075 \text{ V}}{4.5 \text{ A}} = 0.017 \Omega \quad (20)$$

Use 10 m $\Omega$  to allow for ripple-current.

**Inductor Selection L**

$$L = 200 \times \frac{0.01 \Omega}{400 \text{ kHz}} = 5 \mu\text{H} \quad (21)$$

Use 8.2  $\mu\text{H}$ .

**Inductor Ripple Current**

$$\Delta I_{\text{L RIPPLE}} = \frac{3.3 \text{ V}}{400 \text{ kHz} \times 8.2 \mu\text{H}} \times \left( 1 - \frac{3.3 \text{ V}}{14 \text{ V}} \right) = 0.77 \text{ A} \quad (22)$$

**Output Capacitor C<sub>O</sub>**

$$C_O = \frac{2 \times 4.5 \text{ A}}{400 \text{ kHz} \times 0.2 \text{ V}} = 112 \mu\text{F} \quad (23)$$

Use 100  $\mu\text{F}$ .

**Input Capacitor C<sub>I</sub>**

$$C_I = \frac{0.25 \times 4.5 \text{ A}}{400 \text{ kHz} \times 0.5 \text{ V}} = 5.6 \mu\text{F} \quad (24)$$

Use 10  $\mu\text{F}$ , shared between Buck1 and Buck2.

**High-Side MOSFET (TOP\_SW2)**

$$(4.5 \text{ A})^2 \times 0.009 \times (1 + 0.4) \times 0.236 + \left( \frac{14 \text{ V} \times 4.5 \text{ A}}{2} \right) \times (20 \text{ ns} + 20 \text{ ns}) \times 400 \text{ kHz} = 0.56 \text{ W} \quad (25)$$

**Low-Side MOSFET (BOT\_SW2)**

$$(4.5 \text{ A})^2 \times 0.009 \times (1 + 0.4) \times 1 - 0.236) + 0.6 \text{ V} \times 4.5 \text{ A} \times (2 \times 20 \text{ ns}) \times 400 \text{ kHz} = 0.24 \text{ W} \quad (26)$$

## Buck3 Component Selection

### Duty Cycle

$$D = \frac{1.8}{5} = 0.36 \quad (27)$$

### Inductor Selection $L_{\text{BUCK3}}$

$$L_{\text{BUCK3}} = \frac{3.7 \Omega}{400 \text{ kHz}} = 9.25 \mu\text{H} \quad (28)$$

Use 8.2  $\mu\text{H}$ .

### Inductor Ripple Current

$$\Delta I_{\text{RIPPLE}} = \frac{1.8 \text{ V}}{400 \text{ kHz} \times 8.2 \mu\text{H}} \times \left(1 - \frac{1.8 \text{ V}}{5 \text{ V}}\right) = 0.46 \text{ A} \quad (29)$$

### Output Capacitor $C_{\text{O}}$

$$C_{\text{O}} = \frac{2 \times 4.6 \text{ A}}{400 \text{ kHz} \times 0.075 \text{ V}} = 30.7 \mu\text{F} \quad (30)$$

Use 100  $\mu\text{F}$ .

### Input Capacitor $C_{\text{I}}$

$$C_{\text{I}} = \frac{0.25 \times 2.2 \text{ A}}{400 \text{ kHz} \times 0.05 \text{ V}} = 5.76 \mu\text{F} \quad (31)$$

Use 10  $\mu\text{F}$ .

### Internal High-Side MOSFET

$$(2.2 \text{ A})^2 \times 0.28 \Omega \times 0.36 + \left(\frac{5 \text{ V} \times 2.2 \text{ A}}{2}\right) \times (20 \text{ ns} + 20 \text{ ns}) \times 400 \text{ kHz} = 0.58 \text{ W} \quad (32)$$

### Internal Low-Side MOSFET

$$(2.2 \text{ A})^2 \times 0.28 \Omega \times (1 - 0.36) + 0.6 \times 2.2 \text{ A} \times (2 \times 20 \text{ ns}) \times 400 \text{ kHz} = 0.89 \text{ W} \quad (33)$$

## Power Dissipation

The power dissipation is dependent on the MOSFET drive current and input voltage. The drive current is proportional to the total gate charge of the external MOSFET.

### Power Dissipation BUCK1 and BUCK2 (VBUCK1 and VBUCK2)

$$P_{\text{Gate drive}} = Q_{\text{g}} \times V_{\text{VREG}} \times f_{\text{sw}} \text{ (Watts)} \quad (34)$$

Assuming both high and low side MOSFETs are identical in a synchronous configuration, the total power dissipation per BUCK is

$$P_{\text{BUCK1}} = 2 \times Q_{\text{g}} \times f_{\text{sw}} \times V_{\text{VREG}} \text{ (Watts)} \quad (35)$$

### Power Dissipation of the Buck Converter (VBUCK3)

#### High-Side Switch

The power dissipation losses are applicable for positive output currents:

$$P_{\text{HS-CON}} = I_{\text{OUT}}^2 \times R_{\text{DS(on)}} \times (V_{\text{OUT}}/V_{\text{IN}}) \text{ (Conduction losses)} \quad (36)$$

$$P_{\text{HS-SW}} = \frac{1}{2} \times V_{\text{SUP}} \times I_{\text{out}} \times (t_{\text{r}} + t_{\text{f}}) \times f_{\text{SW}} \text{ (Switching losses)} \quad (37)$$

$$P_{\text{HS-Gate}} = 1 \text{ nC} \times f_{\text{sw}} \text{ (Gate drive losses, valid at } V_{\text{VREG}} = 5.8 \text{ V, } V_{\text{SUP}} = 4 \text{ V)} \quad (38)$$

$$P_{\text{HS-Total}} = P_{\text{HS-CON}} + P_{\text{HS-SW}} + P_{\text{HS-Gate}} \quad (39)$$

### Low-Side Switch

The power dissipation losses are applicable for positive output currents.

$$P_{LS\_CON} = I_{OUT}^2 \times R_{DS(on)} \times (1 - V_{OUT}/V_{IN}) \quad (\text{Conduction losses}) \quad (40)$$

$$P_{LS\_SW} = \frac{1}{2} \times V_{SUP} \times I_O \times (t_r + t_f) \times f_{SW} \quad (\text{Switching losses}) \quad (41)$$

$$P_{LS\_Gate} = 1 \text{ nC} \times f_{sw} \quad (\text{Gate drive losses, valid at } V_{VREG} = 5.8V, V_{SUP} = 4V) \quad (42)$$

$$P_{LS\_DIODE} = 2 \times V_f \times I_o \times f_{sw} \times t_{dead} \quad (\text{low side body diode losses during dead time}) \quad (43)$$

$$P_{LS\_Total} = P_{LS\_CON} + P_{L\_SW} + P_{LS\_Gate} + P_{LS\_DIODE} \quad (44)$$

### Linear Regulator (LREG1)

$$P_{LREG1} = (V_{VLR1} - V_{LREG1}) \times I_{OUT} \quad (45)$$

Where

$V_{OUT}$  = Output voltage,  $V_{IN}$  = Input voltage

$I_{OUT}$  = Output current,  $f_{sw}$  = Switching frequency

$t_r$  = rise time of switching node PH3

$t_f$  = fall time of switching node PH3

$V_{VREG}$  = FET gate drive voltage

$V_f$  = Low side FET diode drop (conduction during dead time)

### IC Power Consumption

$$P_{IC} = I_q \times V_{IN} \quad (\text{Watts}) \quad (46)$$

$$P_{Total} = P_{BUCK1 \text{ and } BUCK2} + P_{HS\_Total} + P_{LS\_Total} + P_{LREG1} + P_{IC} \quad (\text{Watts}) \quad (47)$$

**Table 5.**

	BUCK 1 AND BUCK 2	BUCK 3	COMMENTS
Duty cycle D	$D = \frac{V_O}{V_I}$	$D = \frac{V_O}{V_I}$	Buck 3 will be powered from Buck 1 or Buck 2
Current limit sense resistor RS	$R_S = \frac{0.075}{1.25 \times I_{Omax}}$	Not Applicable	Choose current limit of 25% more than max load
Inductor selection L	$L = \frac{200}{f_{SW}} \times R_S$	$L = \frac{3.7}{f_{SW}}$	Rs is chosen based on current limit set for the application.
Inductor ripple current	$\Delta I_{LRIIPPLE} = \frac{V_O}{f_{SW} \times L} \times \left(1 - \frac{V_O}{V_I}\right)$	$\Delta I_{LRIIPPLE} = \frac{V_O}{f_{SW} \times L} \times \left(1 - \frac{V_O}{V_I}\right)$	Typically the $\pm$ inductor ripple current is 25% of max load current
Output Capacitor Co	$C_O = \frac{\Delta I_O}{4 \times GBW \times \Delta V_O}$	$C_O = \frac{\Delta I_O}{4 \times GBW \times \Delta V_O}$	Also consider the ESR of the output capacitor influences output voltage ripple due to load steps
Input Capacitor CIN	$C_{IN} = \frac{0.25 \times \Delta I_{O MAX}}{f_{SW} \times \Delta V_I}$	$C_{IN} = \frac{0.25 \times \Delta I_{O MAX}}{f_{SW} \times \Delta V_I}$	Based Input capacitor value on input voltage ripple desired
Soft Start CSS	$C_{SS} = \frac{1 \mu A \times \Delta t}{0.8}$	$C_{SS} = \frac{1 \mu A \times \Delta t}{0.8}$	Chose the soft start time required $\Delta t$ and then calculate C <sub>ss</sub>
Bootstrap capacitor CBoot	$C_{BOOT} = \frac{Qg}{\Delta V}$	$C_{BOOT} = \frac{Qg}{\Delta V}$	Chose based on the desired amount of ripple based on FET gate charge and operating Vin
Compensation Resistor for GBW	$R3 = \frac{GBW \times 2 \pi \times C_O}{gm \times K_{CFB} \times \beta}$	$R3 = \frac{GBW \times 2 \pi \times C_O}{gm \times Gm3 \times \beta}$	To determine resistor R3 assume $GBW \approx f_{sw}/5$ to $f_{sw}/20$
Compensation Capacitor for zero	$C1 = \frac{1}{2 \pi \times R3 \times 0.1 \times GBW}$	$C1 = \frac{1}{2 \pi \times R3 \times 0.1 \times GBW}$	C1 can be also increased 2x for faster small signal settling at expense of large step response (slew rate on COMPx).
Compensation Capacitor for second pole	$C2 = \frac{1}{\pi \times f_{SW} \times R3}$	$C2 = \frac{1}{\pi \times f_{SW} \times R3}$	The value of C2 is also critical for buffering the noise on COMPx pin and so the value of capacitance is a trade off between noise immunity and phase margin.

Table 5. (continued)

	BUCK 1 AND BUCK 2	BUCK 3	COMMENTS
Pole at low frequency with high DC gain	$f_{P1} = \frac{1}{2 \pi \times C1 \times R_{OUT\_OTA}}$	$f_{P1} = \frac{1}{2 \pi \times C1 \times R_{OUT\_OTA}}$	$R_{OUT\_OTA} = 1M\Omega$ min
Zero at Control loop pole related to Output filter LC	$f_{Z1} = \frac{1}{2 \pi \times C1 \times R3}$	$f_{Z1} = \frac{1}{2 \pi \times C1 \times R3}$	Place zero at $0.05...0.1 * GBW$ (see comment on C1 above).
Second pole for type 2a	$f_{PZ} = \frac{1}{2 \pi \times C2 \times R3}$	$f_{PZ} = \frac{1}{2 \pi \times C2 \times R3}$	Place second pole at or below half switching frequency $f_{sw}$ observing distance to GBW.

### Power Dissipation De-Rate Profile 32 pin HTTSOP package with power PAD

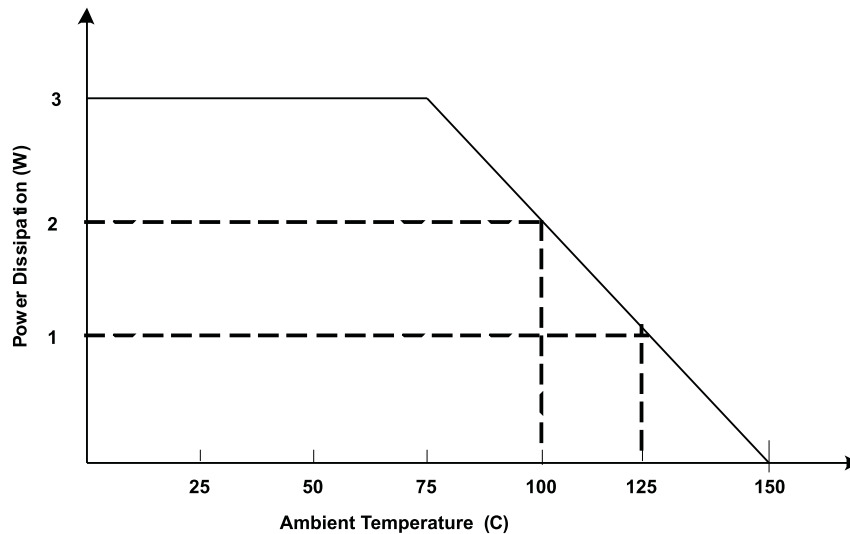


Figure 21. Power dissipation de rating profile based on high K Jedec PCB

### PCB Layout Guidelines

#### Grounding and PCB Circuit Layout Considerations

1. Connect the drain of TOP\_SW1 and TOP\_SW2 together with +ve terminal of the input capacitor  $C_{OUT1}$ . The trace length between these terminals should be short.
2. The Kelvin current sensing for the shunt resistor should have minimum trace spacing and routed together. Any filtering capacitors for noise should be placed near the IC pins.
3. The resistor divider for sensing output voltage is connected between the +ve terminal of the respective output capacitor  $C_{BUCK1}$  or  $C_{BUCK2}$  or  $C_{BUCK3}$  and the IC signal ground. These components and the traces should not be routed near any switching nodes or high current traces.

#### Other Considerations

1. Separate IC signal ground and power ground terminals (GND and PGNDx) pins. Use a star ground configuration if connecting to non ground plane system. Use tie-ins for EXTSUP capacitor, compensation network ground and voltage sense feedback ground networks to this star ground
2. Connect compensation network between compensation pins and IC signal ground. Connect the oscillator resistor (frequency setting) between the RT pin and IC signal ground. These sensitive circuits should NOT be located near the dv/dt nodes; these include the gate drive outputs, phase pins and boost circuits (bootstrap).
3. Reduce the surface area of the high current carrying loops to a minimum, by ensuring optimal component placement. Ensure the bypass capacitors are located as close as possible to their respective power and ground pins.



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPS43340QPHPQ1	PREVIEW	HTQFP	PHP	48	250	TBD	Call TI	Call TI	
TPS43340QPHPRQ1	ACTIVE	HTQFP	PHP	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

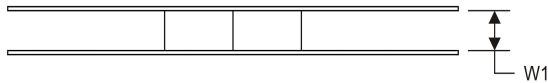
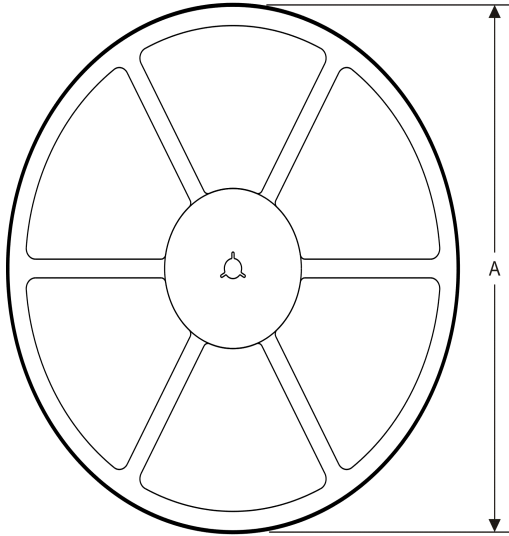
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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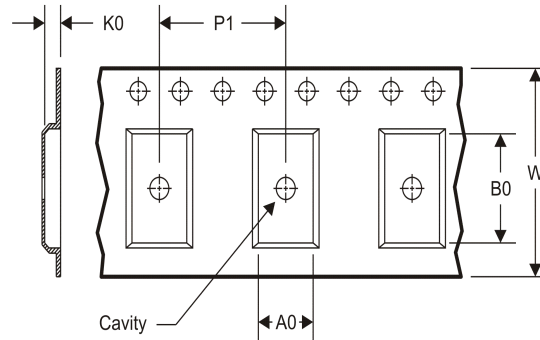
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



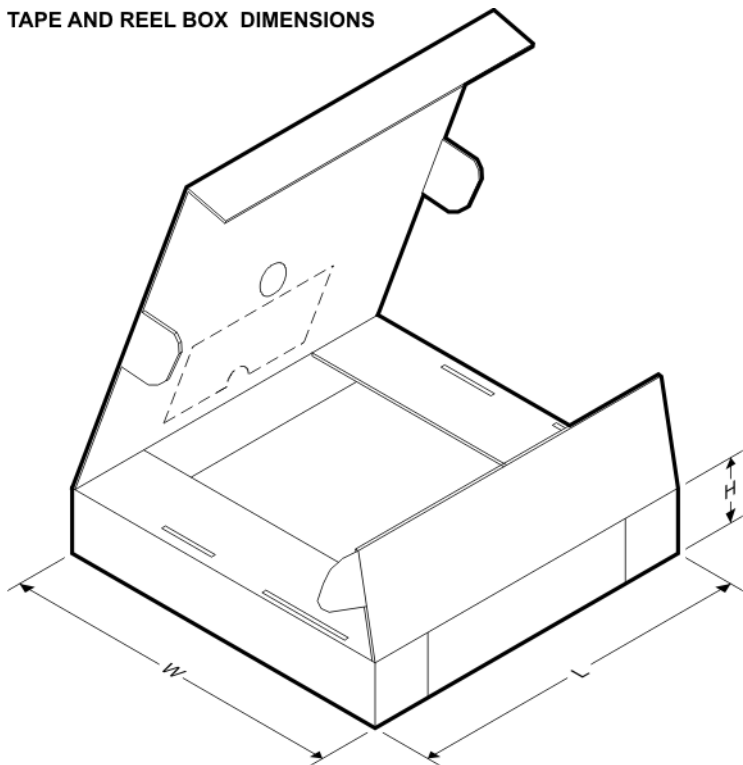
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS43340QPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**

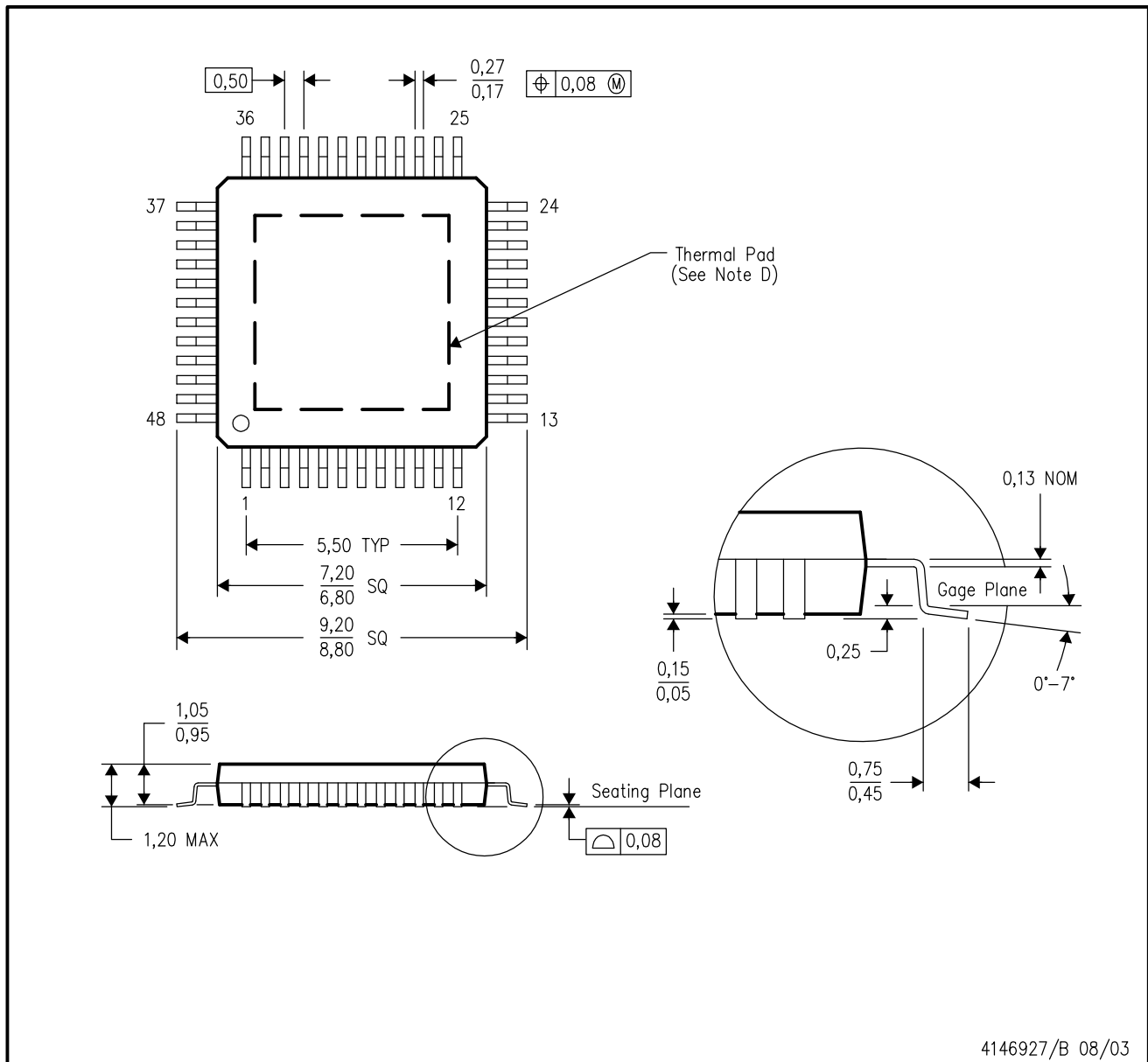


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS43340QPMPRQ1	HTQFP	PHP	48	1000	346.0	346.0	33.0

PHP (S-PQFP-G48)

PowerPAD™ PLASTIC QUAD FLATPACK



4146927/B 08/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

# THERMAL PAD MECHANICAL DATA

PHP (S-PQFP-G48)

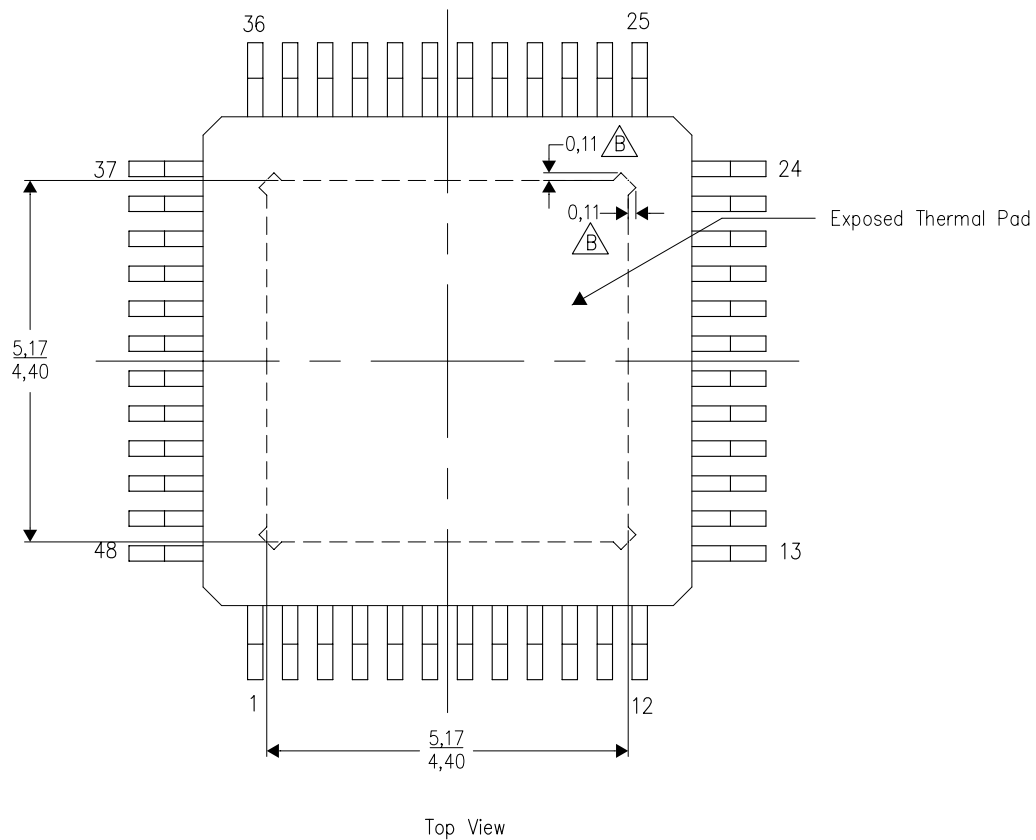
PowerPAD™ PLASTIC QUAD FLATPACK

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).


The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206329-7/M 01/11

NOTE: A. All linear dimensions are in millimeters

 Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

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